ATTACHMENT 2. FLIGHT DATA INPUT/OUTPUT (FDIO) SYSTEM, SOFTWARE INTERFACE CONTROL DOCUMENT (NAS-MD-581)

PAGE CONTROL CHART

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NATIONAL AIRSPACE SYSTEM

En Route

INTERFACE CONTROL DOCUMENT (ICD)

FLIGHT DATA INPUT/OUTPUT PROGRAM (FDIO)

SOFTWARE INTERFACE CONTROL DOCUMENT (SICD)

Model A5f1.0

NAS-MD-581

June 2000

Operational Support
National En Route Automation Division, AOS-300
Federal Aviation Administration
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	July 1995		Refer to Order 6130.1, Chapter 243.
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	June 1999	N20716, N20442	Refer to Order 6130.1, Chapter 253.
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1.0 INTRODUCTION

This document describes the hardware interfaces as well as the firmware necessary for the control of the Flight Data Input/Output (FDIO) system. The FDIO system consists of three subsystems, the Central Control Unit (CCU), the Printer Control Unit (PCU), and the Remote Control Unit (RCU). These control units provide communication paths between the National Airspace System (NAS) Host computer and FDIO's Input/Output (I/O) devices consisting of Replacement Alphanumeric Keyboards (RANK), Cathode Ray Tubes (CRT), and Replacement Flight Strip Printers (RFSP) that will be used for entering, displaying, and printing NAS messages. These will allow for communicating NAS messages between the Air Route Traffic Control Center (ARTCC) and remote sites.

The FDIO system will perform these communication tasks by using the following three interface channels that communicate with other system components (reference figure 1-1):

① General Purpose Output (GPO) interface channel at the CCU and PCU

② General Purpose Input (GPI) interface channel at the CCU and PCU

③ Peripheral device interface at the PCU and RCU.

Control of the GPI and GPO interfaces is shared by both FDIO firmware and Host software. Control of the peripheral device interface is primarily the responsibility of the Bus Connector (BC) with some protocol operations performed by the peripheral device.

1.1 PURPOSE OF DOCUMENT

The Software Interface Control Document (SICD) describes the communication interfaces between the FDIO system and the Host, as well as between the FDIO system and its peripheral devices. It provides detailed descriptions of the hardware characteristics, device addressing, interface channel control commands, interface channel signal sequencing, and message formats. The SICD serves as the design document for all FDIO interfaces and was used to develop test cases to verify the completeness and accuracy of the design. The SICD can also be used by third parties to gain an understanding of the system interfaces, by programmers for coding the firmware, and by maintenance people following system delivery.

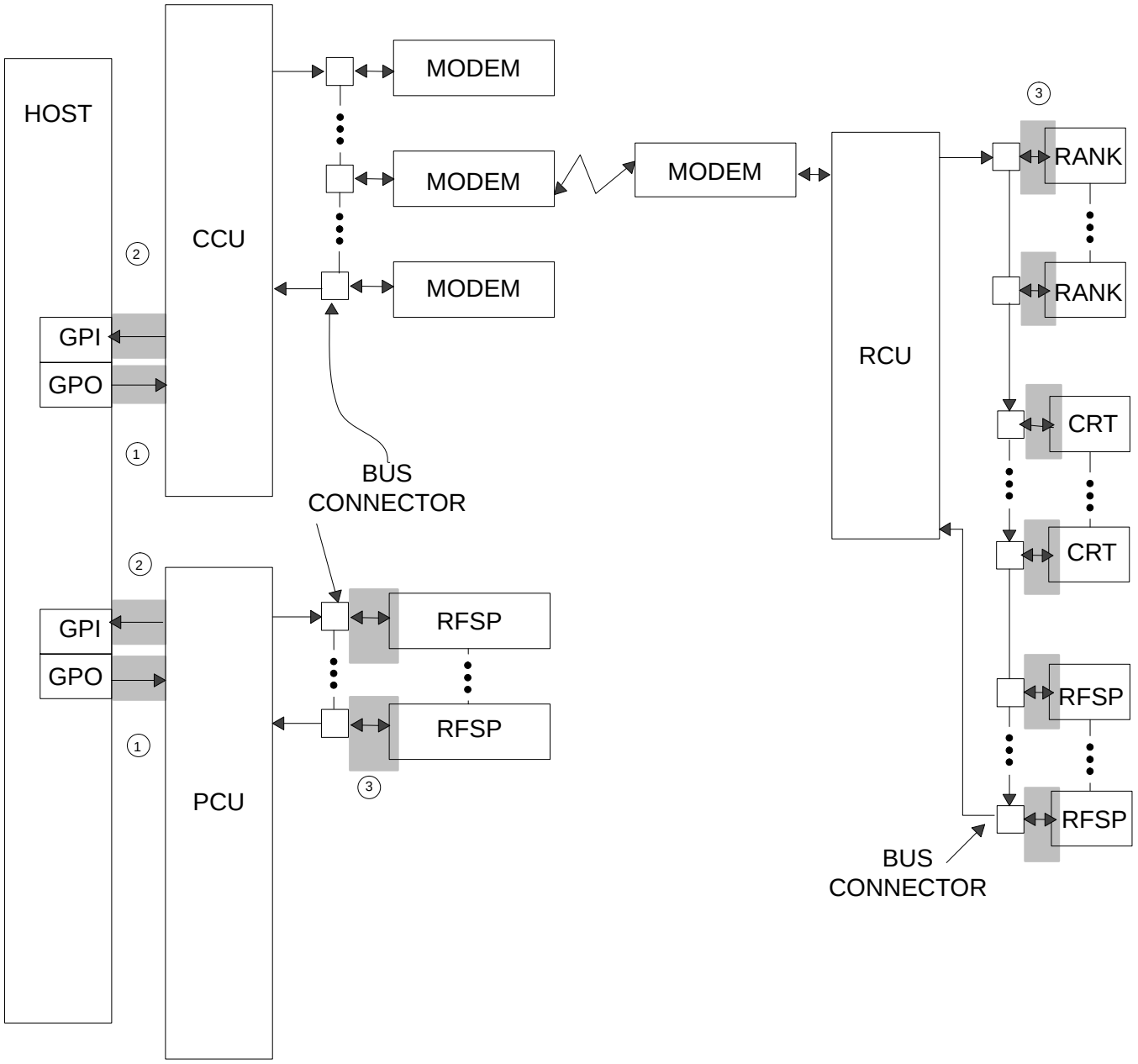


FIGURE 1-1. FDIO INTERFACE CHANNELS

1.2 ORGANIZATION OF THE SICD

This document is a single volume consisting of six sections and four appendixes:

Sections	Title
1.0	Introduction — This section contains an introduction to the SICD.
2.0	Hardware Characteristics — This section describes each of the three interfaces with regard to its physical properties as well as its relationship with the controlling firmware.
3.0	Startup, Startover Operation — This section describes how the interface channels are initially set up and what procedures must be followed to reinitialize them.
4.0	FDIO Message Descriptions — This section describes the types and formats of the FDIO messages and what information they contain.
5.0	Message Transfers Over GPI and GPO Interfaces — This section describes the NAS messages that are communicated over the GPI and GPO channels.
6.0	Data Transfers Over Peripheral Device Interface — This section describes the messages that are used to communicate between the BC and its peripheral devices (RANK, CRT, or RFSP).

Appendixes	Title
A	System Interrupt Structure — This appendix describes the internal FDIO interrupt structure.
B	FDIO Character Set Definition — This appendix describes the character set used by FDIO.
C	FDIO Error Messages — This appendix lists all FDIO error messages.
D	FDIO Master Acronym Glossary

1.3 DEFINITIONS

1.3.1 Acronym Glossary

Appendix D contains the FDIO Master Acronym Glossary.

1.3.2 Terminology Glossary

This paragraph lists terms that have a specific definition within the context of this document.

Advanced Data Communications Control Protocol (ADCCP) frame — a data structure of fields made up of bits and organized according to the ADCCP standard format that is transmitted over the local area network.

Buffer — a set of memory locations used for temporary storage.

Bus Connector (BC) — a custom designed board that provides the interface between the PCU or RCU and a peripheral device, or between the CCU and the modem.

Control Unit — one of the redundant units of a CCU or PCU control unit pair or a non-redundant RCU.

Control Unit Pair — a set of two control units, A and B where one unit is the primary control unit and the other is the secondary.

Firmware — the program used to control the operation of the FDIO system that is stored in Programmable Read Only Memory (PROM).

Inward Message — a message characterized by a general flow from the peripheral devices towards the Host.

Frame Check Sequence (FCS) — an ADCCP field that allows the validation of the address, control, and information fields of the ADCCP frame.

Line — refers to an interface signal consisting of physical wire, be it twisted pair or coax.

Mailbox — a location in memory where a single intertask communication message is placed.

Message — a sequence of characters containing data or control information that causes an operation to be performed by the unit receiving the message.

Outward Message — a message characterized by a general flow from the Host towards the peripheral devices.

Peripheral Device — an RFSP, CRT, or RANK.

Primary Control Unit — one of two redundant control units (CCU or PCU) that is actively transmitting information to and receiving information from the Host and FDIO peripheral devices.

Queue — a location in memory that provides a mechanism for passing messages; more than one message may be placed on a queue.

Queue Entry — a collection of four bytes, usually a pointer to an FDIO message.

Secondary Control Unit — one of two redundant control units (CCU or PCU) that is processing information received from the Host and FDIO peripheral devices (downloaded from the primary via Intercomputer Link (ICL), but is not transmitting the backup control unit for the primary.

Text Acknowledge — a message sent to the Host, indicating that a Text message (see paragraph 5.1.1) has successfully been printed (displayed) at its intended device or at its backup device.

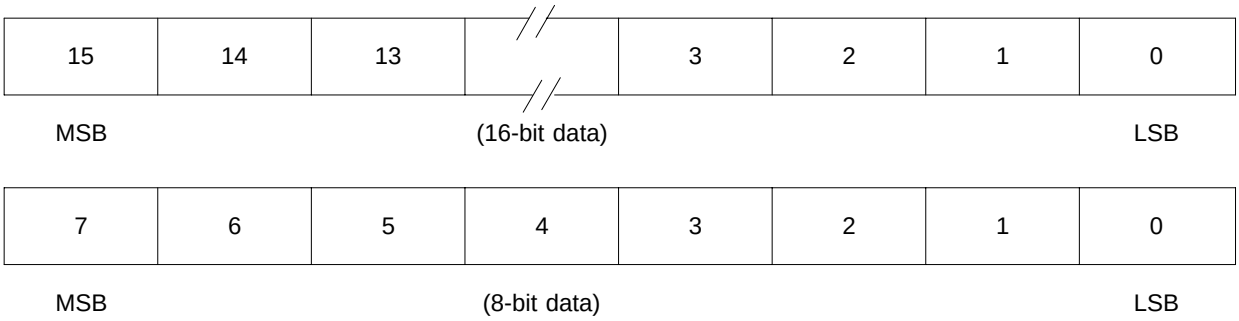
Text Acknowledge with Error — a message sent to the Host, indicating that a Text message could not be printed (displayed) at its primary or backup device.

Watchdog Timer — a hardware timer used to ensure that a firmware operation does not exceed its allowable time in which it has to operate.

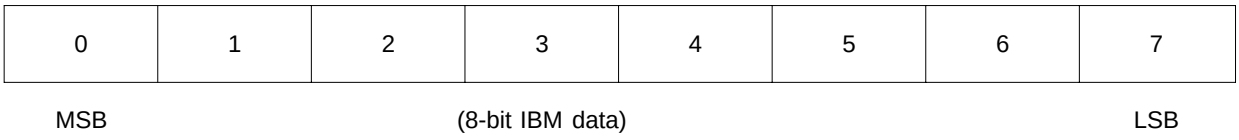
1.3.3 Data Format

The FDIO system recognizes two types of formats for representing data, one utilized by internal FDIO hardware and firmware, the other being the IBM format.

1.3.3.1 Internal FDIO Data Format. FDIO firmware used both 8 and 16 bit wide data. The following conventions are used when referencing internal FDIO formats:



1.3.3.2 IBM Format. The 8-bit data format used by IBM for information transferred over the GPI or GPO interface is numbered differently than the internal FDIO format. The following convention is used when referencing the IBM format:



1.4 APPLICABLE DOCUMENTS

FAA-E-271 1 A	FIDO Specification
FAA-SRDS-140-SDS-1	Software Documentation Standards for Program Development
NAS-MD-31 1	Message Entry and Checking
NAS-MD-314	Local Outputs
NAS-MD-315	Remote Outputs
FDIO-51G1	Overall Computer Program Description (OCPD)
FDIO-51G2	Computer Program Functional Specification (CPFS)
FDIO-51G4	Program Design Specification (PDS)
FDIO-PPSP-001 1	Document Modification Procedure

1.5 PROCEDURES FOR MODIFICATION

Modifications to this document shall be in accordance with FDIO-PPSP-0011.

1.6 INTERFACE OVERVIEW

1.6.1 GPI and GPO Interfaces

The GPI and GPO interfaces provide a means of communicating between the FDIO system and the Host via the Peripheral Adapter Module Replacement Item (PAMRI) at the Host. The GPI and GPO interfaces send and receive eight bits of data plus parity in a bit parallel, byte serial format. The link protocol is governed by the Device Control Lines (DCL) of the GPI interface and the Device Status

Lines (DSL) of the GPO interface, as well as the handshake lines. Messages containing textual information destined for RFSPs and CRTs, as well as other control information are communicated between the Host and the FDIO system over these interfaces.

1.6.2 Peripheral Device Interface

BCs on the PCU or RCU Local Area Network (LAN) are connected to asynchronous peripheral devices such as RFSPs, CRTs, or RANKs through a serial RS-422 interface. The BC determines the type of peripheral device attached to it by reading the peripheral status byte. The BC transmits the message received from the control unit to its peripheral device via the peripheral device interface, checks for errors, and performs appropriate error recovery. The BC also accepts data characters entered at a RANK and transmits them to the RCU.

2.0 HARDWARE CHARACTERISTICS

This section describes each of the hardware interfaces. Included is a description of the relationship between the hardware and the controlling firmware.

2.1 GPO INTERFACE

Figure 2-1 shows the GPO interface within the FDIO system.

The CCU and PCU receive messages from the Host GPO adapter via the GPO interface. Each CCU and PCU consist of two control units, a primary control unit and a secondary control unit which are configured as a redundant pair. The GPO interface from the Host is connected in parallel to both the primary and secondary control units. Both control units receive messages from the Host over the GPO interface (see figure 2-2).

2.1.1 General Description

The PCU and CCU control units receive messages from the Host in bit parallel, byte serial fashion, over the GPO interface. The GPO interface consist of eight data lines, a parity line, handshake lines, and status lines. The FDIO system can accept input data at a maximum rate of approximately 3,500 bytes-per-second (bps) over the GPO interface. Table 2-1 provides a list and description of the physical GPO interface lines.

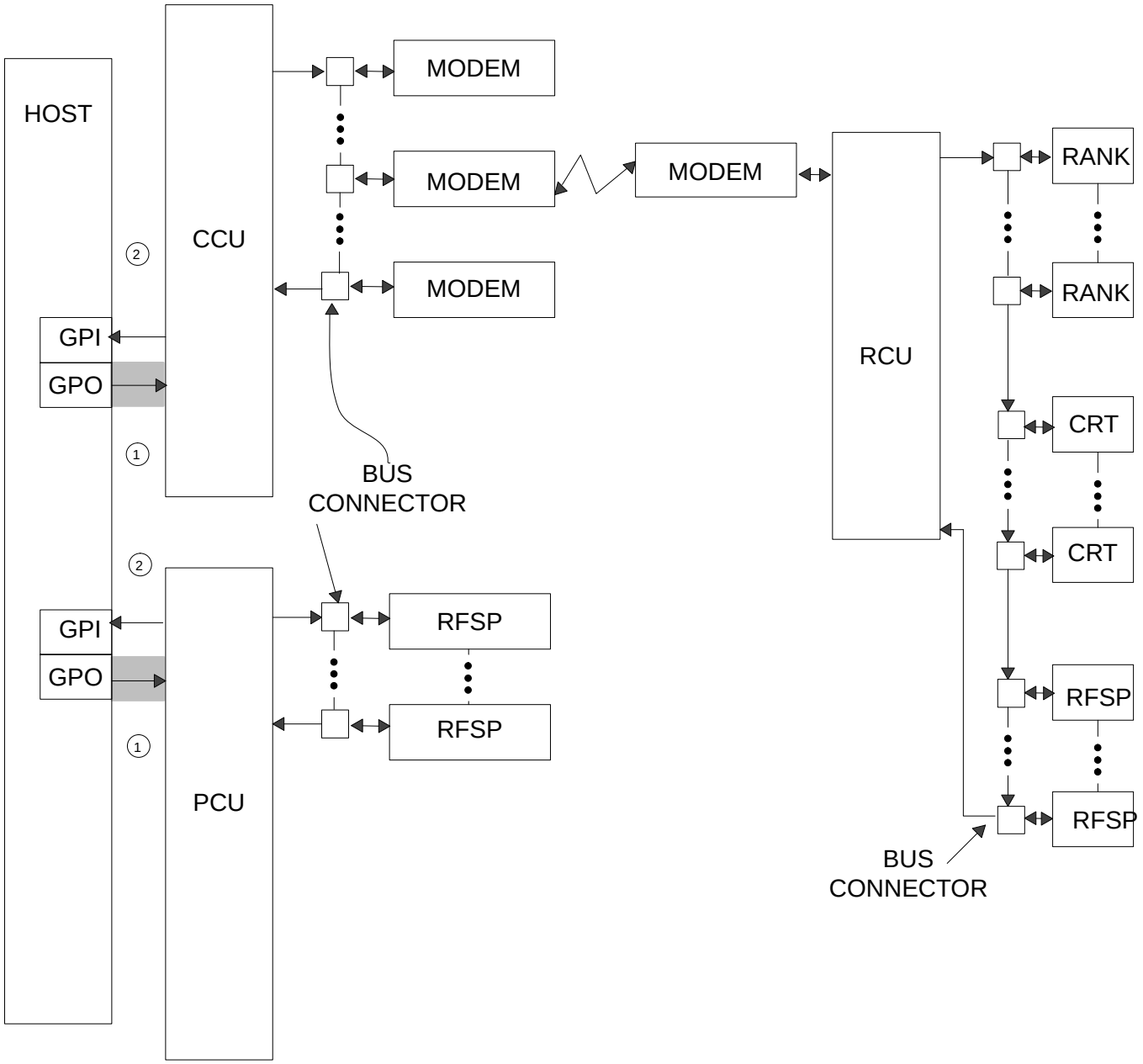
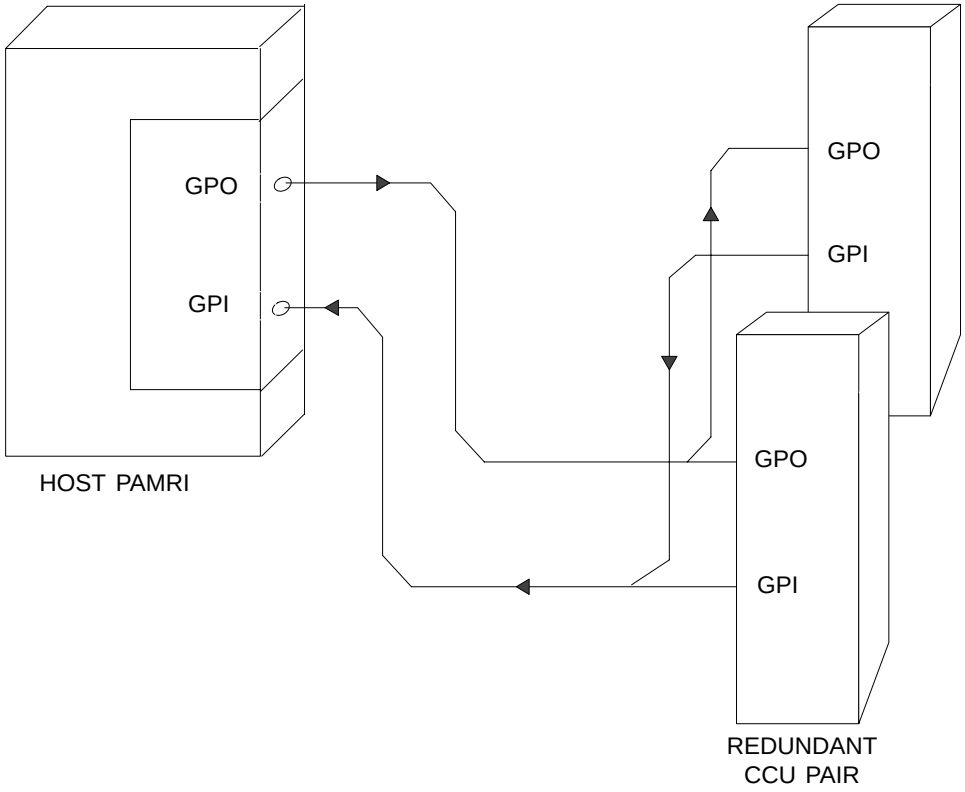


FIGURE 2-1. GPO INTERFACE



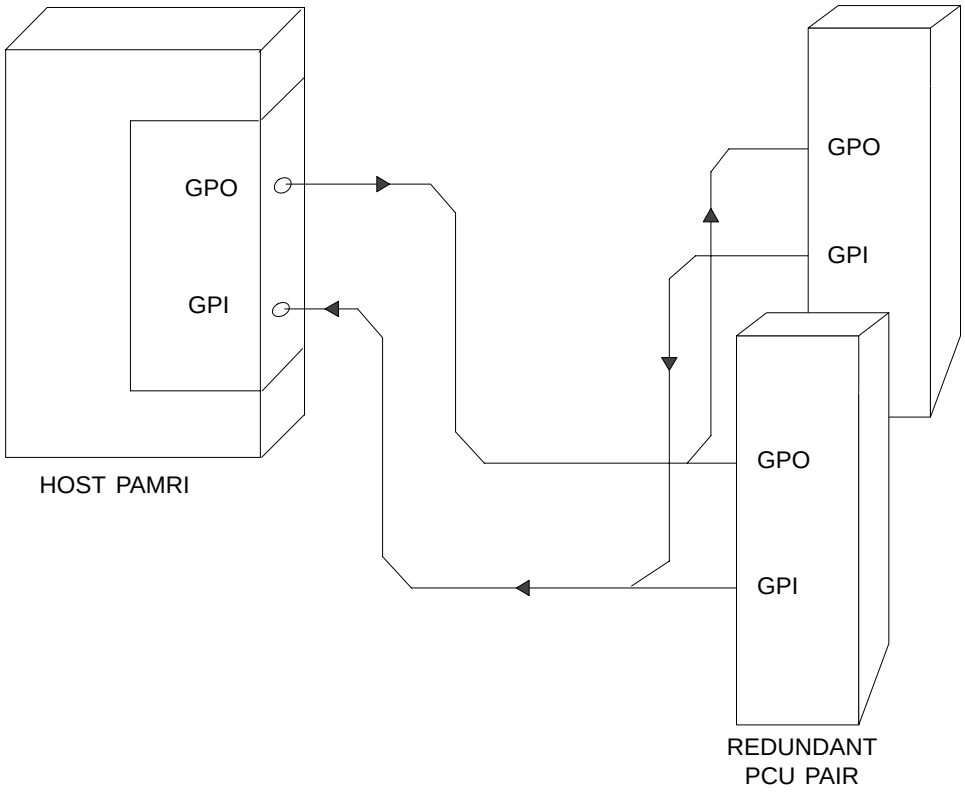


FIGURE 2-2. HOST (PAMRI) — FDIO INTERCONNECTION

TABLE 2-1. GPO INTERFACE SIGNAL DEFINITION

Line	Function [note 1]
DATA LINES	
GPO data 0 (D0)	most significant data bit
GPO data 1 (D1)	
GPO data 2 (D2)	
GPO data 3 (D3)	[Data is in 8-bit IBM format]
GPO data 4 (D4)	
GPO data 5 (D5)	
GPO data 6 (D6)	
GPO data 7 (D7)	least significant data bit
GPO parity	parity bit added to data bits
HANDSHAKE LINES [note 2]	
Adapter Select	IBM is ready to communicate via GPO
GPO I/O Request	CCU/PCU is ready to receive a character
GPO Adapter Response	character available from Host
GPO EOM	End Of Message
DEVICE STATUS LINES [note 2]	
Device Inoperative	CCU/PCU is available to receive data from the Host [note 3]
Device Status Line 3 (DSL3)	CCU/PCU has received a parity error
Device Status Line 5 (DSL5)	CCU/PCUs receive buffer has overflowed
Device Status Line 6 (DSL6)	CCU/PCU requests that the Host resend the message

NOTES

1. All interface signals are active when they are high.
2. These lines are referred to in the PAMRI manual as control lines.
3. The device inoperative line is inactive (high) when FDIO is operational (i.e., available to receive data from the Host).

2.1.1.1 GPO Block Diagram. The GPO interface consists of the following functional building blocks as shown in figure 2-3:

a. Receive Buffers — This section contains the circuitry that buffers the GPO input signals.

b. Parallel Peripheral Interface — This circuit consists of a Parallel Peripheral Interface (PPI) chip (8255) and is utilized to read the input data and make it available to the control unit firmware.

c. Parity Check Logic — This section tests the 8-bit input data for correct parity and indicates to the control unit firmware if there is an error.

d. Handshake Logic — This section contains the circuitry that controls the sequence of events required to interface with the Host GPO adapter. In addition, this circuitry invokes the GPO hardware interrupt that is sent to the Priority Interrupt Controller (PIC).

e. Transmit Buffers — This section contains the circuitry that buffers and transmits the handshake and status signals to the Host GPO adapter.

2.1.2 Device Addressing

2.1.2.1 GPO Parallel Peripheral Interface. The GPO PPI contains three 8-bit I/O ports, A, B, and C which are utilized by the GPO interface to input the GPO data character as well as control the GPO interface logic. The GPO PPI is a memory mapped device with address assignments shown in table 2-2.

TABLE 2-2. GPO PPI ADDRESSING

Memory Address	Function
F900	PORT A — output: controls GPO handshake logic
F901	PORT B — input: read 8-bit GPO data character
F902	PORT C (lower 4 bits) — input: GPO handshake status (upper 4 bits) — output: controls GPO handshake logic
F903	CONTROL REGISTER output

2.1.2.2 Priority Interrupt Controller. The PIC receives the GPO interrupt generated by the GPO handshake logic. It is addressed as an I/O device and is assigned addresses E0 and E1 hex. See appendix A for complete information regarding PIC operation.

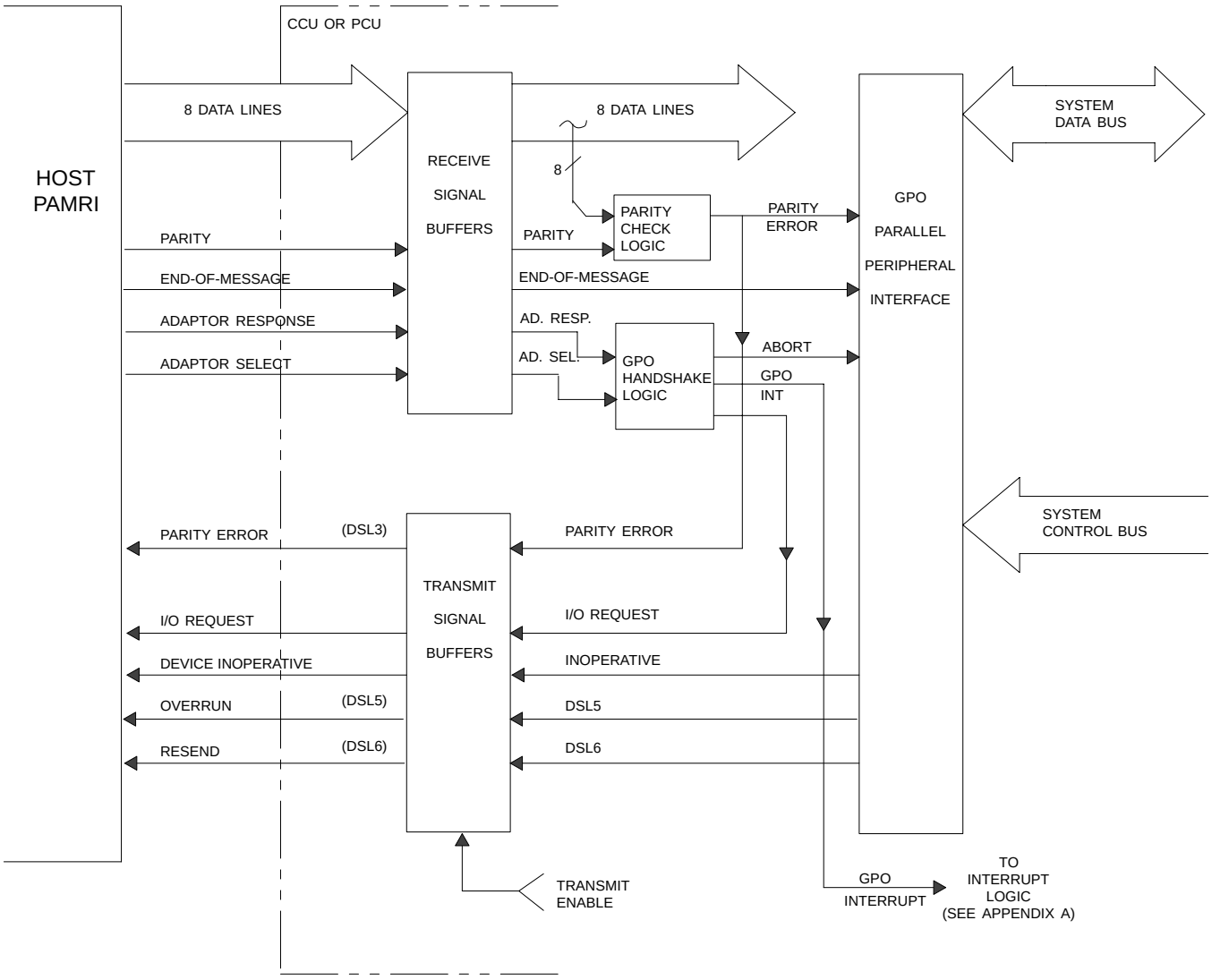


FIGURE 2-3. GPO BLOCK DIAGRAM

2.1.3 GPO Interface Control Commands

2.1.3.1 GPO Interface Setup Commands. Before GPO operation can commence, the GPO PPI controller must be initialized to place the three 8-bit I/O ports into the correct operating mode. In addition, the PIC must be set up to recognize GPO interrupts.

2.1.3.1.1 GPO PPI Initialization. The GPO PPI setup requirements are as follows:

a. Port A programmed to output mode

b. Port B programmed to input mode

c. Port C (upper 4 bits) programmed to output mode

d. Port C (lower 4 bits) programmed to input mode

e. Device Inoperative set inactive (high)

f. DSL3, DSL5, and DSL6 status lines set inactive (low)

g. GPO handshake lines initialized

The GPO PPI setup will be performed by writing to its control register, and by initializing the output bits as follows:

Command Operation	Command Address	Command Contents (binary)	Command Description
OUTPUT	F903	10000011	Set port A to output mode Set port B to input mode Set lower port C to input Set upper port C to output
OUTPUT	F900	11000011	Initialize port A: DSL3, 5, 6 = inactive (low) Initialize GPO handshake logic
OUTPUT	F902	00000000	Initialize port C (upper 4 bits): Initialize GPO handshake logic

2.1.3.1.2 PIC Initialization. The PIC consists of an 8259A Large Scale Integration (LSI) device whose setup is described in appendix A.

2.1.3.2 GPO Operational Commands. GPO operational commands involve the setting of control bits and the reading of status bits at certain points within the GPO receive operation. In addition, the PIC must be instructed to update its internal interrupt status following each GPO interrupt.

2.1.3.2.1 GPO Control Bits. The GPO hardware circuitry is controlled by the GPO firmware resident in the control unit (CCU or PCU) via the GPO PPI controller. Port A and the upper four bits of port C are configured as outputs providing twelve control bits (not to be confused with the DCL lines).

The following control bits are available by writing an 8-bit control word to port A of the GPO PPI, memory address F900 (hex):

7	6	5	4	3	2	1	0

MSB LSB

Bit	Description
0	GPOENB/ — When active (low), this signal enables the GPO transmit buffers of the primary control unit and disables (=1) DEVICE INOPERATIVE.
1	GPOINTACK/ — When pulsed low, this signal clears the GPO IOREQ handshake signal.
2	MSGXFREN — When active (high), this signal allows the GPO IOREQ handshake signal to be set when GPO ADAPTER RESPONSE drops low.
3	GPODSL3 — When active (high), this signal causes the DSL3 interface line to go high (indicates a receive parity error).
4	GPODSL5 — When active (high), this signal causes the DSL5 interface line to go high (indicates a receive overflow error).
5	GPODSL6 — When active (high), this signal causes the DSL6 interface line to go high (indicates a resend request).
6	CMDSWENB/ — Used by the fail safe circuit.
7	GPOABORTENB — When active (high), this signal enables the GPO abort detection circuit.

NOTE

A slash (/) as part of the signal name indicates the signal is active when it is at a logical low level.

The following control bits are available by writing an 8-bit control word to port C of the GPO PPI, memory address F902 (hex):

7	6	5	4	X	X	X	X

MSB LSB

The setting of bits 0 to 3 do not matter, since the lower four bits of port C are inputs only and not affected by an output command.

Bit	Description
4	WD — Used by the fail safe circuit.
5	GPOTEST — When active (high), this signal puts the GPO data buffers into loop-back mode.
6	GPOTA — Used with GPOTB to select one of four input patterns during GPO loop-back testing.
7	GPOTB — See bit 6 GPOTA.

2.1.3.2.2 GPO Data and Status Bits. Port B and the lower four bits of port C are configured as inputs and allow for the reading of the eight GPO data bits in addition to four status bits (not to be confused with the Device Status Lines (DSL).

The 8-bit GPO data character is available by reading port B of the GPO PPI, memory address F901 (hex):

7	6	5	4	3	2	1	0

MSB LSB

Bit	Description
0-7	GPOD0-GPOD7 — 8-bits of GPO data.

The following four status bits are available by reading port C of the GPO PPI, memory address F902 (hex):

X	X	X	X	3	2	1	0

MSB LSB

Bit	Description
0	IORQIN — This status bit indicates the state of the redundant Control Unit's (CU) GPO IOREQ handshake line, and is used for synchronizing purposes.
1	GPOABORT — When active (high), this signal indicates that a GPO abort condition exists.
2	BADGPOPAR — When active (high), this signal indicates the GPO data byte received contained bad parity.
3	GPOEM — This bit indicates the state of the GPO End of Message (EOM) interface line.

Port C bits 4-7 have no meaning since they are programmed as outputs only.

2.1.3.2.3 PIC Operational Commands. The PIC must be informed when the GPO interrupt service routine is being exited. This will reset the 8259A PIC controllers internal-in-service register and enable other interrupts to occur. This is accomplished by executing the following command:

Command	Address	Data	Command Description
OUTPUT	00EO	20 (hex)	Perform end-of-interrupt operation

2.1.4 GPO Read Signal Sequences

The following 6 subsections describe the GPO signal sequences:

1. 2.1.4.1 GPO Initialization Signal Sequences
2. 2.1.4.2 GPO Normal Operation Signal Sequences
3. 2.1.4.3 GPO Abort Operation Signal Sequences
4. 2.1.4.4 GPO Parity Error Signal Sequences
5. 2.1.4.5 GPO Overrun Error Signal Sequences
6. 2.1.4.6 GPO Resend Signal Sequences

Figures 2-4 through 2-8 are signal sequence diagrams and provide additional information pertaining to the relative timing of the different GPO signals and operations. They do not show absolute timing relationships and should not be used for that purpose. The numbers in circles correspond to the descriptions referenced in the text.

2.1.4.1 GPO Initialization Signal Sequences. The initialization of the GPO hardware proceeds in two stages. The first part occurs at power-up or reset, when the operating mode of the GPO PPI controller is established, the handshake logic is reset and the status lines DSL3, DSL5, DSL6 and DEVICE INOPERATIVE are cleared (=0). In addition, the transmit buffers are disabled by disabling GPOENB/ (=1).

The second part of the GPO Initialization is performed at a later time when it is known to the control unit whether it will operate as a primary or secondary unit (see FDIO-51G4 for details). If the control unit is a primary unit, the following lines are initialized: DEVICE INOPERATIVE set inactive (=1), MSGXFREN enabled (=1) and GPOINTACK/ (pulsed low). In addition, the GPO transmit buffers are enabled by activating GPOENB/ (=0). If the control unit is a secondary unit, it will activate the same lines as the primary control unit, however, it will not activate GPOENB/.

Pulsing the internal signal GPOINTACK/ resets the GPO IOREQ handshake signal. Enabling the signal MSGXFREN allows GPO IOREQ to become active when the Host activates ADAPTER SELECT. The function of the status line DEVICE INOPERATIVE is to indicate to the Host that FDIO is ready, while the status lines DSL3, DSL5, and DSL6 are used to indicate exceptional conditions (see following sections). The reason GPOENB/ is initially inactive during initialization is to prevent the hardware from creating transient signals on the interface lines during power-up.

2.1.4.2 GPO Normal Operation Signal Sequences. Refer to figure 2-4 for signal sequences.

GPO NORMAL OPERATION SIGNAL SEQUENCE

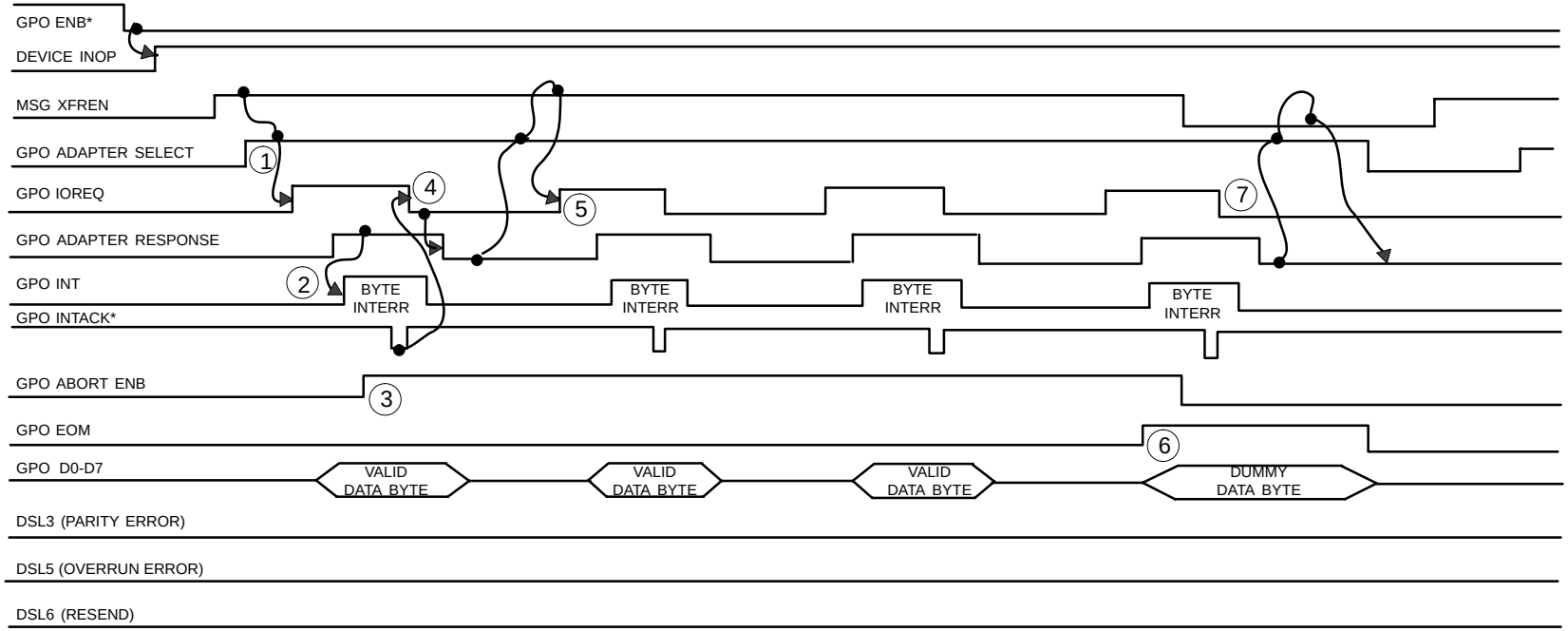


FIGURE 2-4. NORMAL GPO SIGNAL SEQUENCE DIAGRAM

As a result of the GPO Initialization process, DEVICE INOPERATIVE is disabled (=1) which informs the Host that FDIO is ready for operation. The Host will raise the interface line ADAPTER SELECT when it has a message to send (1). When this line is active and the internal line MSGXFREN has been raised, the GPO hardware will raise the handshake line GPO IOREQ. At this time, the Host will place 8 bits of data onto the data lines GPO DATA0-GPO DATA7, generate odd parity on GPO PARITY and will subsequently raise the handshake line GPO ADAPTER RESPONSE. This will cause the GPO handshake logic to raise the interrupt line GPOINT (2) which will invoke the GPO interrupt firmware.

When invoked, the GPO interrupt firmware will check if any special conditions exist. These include EOM and aborted message conditions as well as the occurrence of a parity error. Special conditions are described in the following paragraphs.

If no special conditions exist, a normal byte transfer is assumed. In this case, the GPO Interrupt Handler checks if the data byte is the first byte of the message. If the data byte is the first byte of the message, the internal line GPOABORTENB is raised (3). This will allow the hardware to generate an abort interrupt if the Host drops ADAPTER SELECT during the remainder of the message (i.e., without presenting the EOM signal). Next, the current length of the message is checked against the maximum message length. If the message is about to exceed this maximum, the Host is notified by raising the appropriate status line (see paragraph 2.1.4.5). If no overrun condition exists, the data byte is accepted. When the data byte has been stored, the GPO Interrupt Handler pulses GPOINTACK/ low. This will clear the GPO IOREQ interface handshake line (4).

Both the primary and secondary control unit are performing the GPO handshake operation with the Host. The secondary receives the GPO characters in the same manner in which the primary does, except that any and all output signals (i.e., GPO IOREQ, etc.) from the secondary are disabled, and do not reach the Host. In order to maintain byte synchronization with the secondary control unit, the GPO Interrupt Handler in the primary control unit must not reset its GPO IOREQ until after the secondary has performed the operation. The status bit IORQIN reflects the state of the redundant control units GPO IOREQ line (the handshake logic of the secondary continues to operate but the outputs are electronically terminated and do not reach the GPO interface). By monitoring this line, the primary can delay resetting its GPO IOREQ signal (which is what the Host sees) until the secondary has completed the operation.

When the Host detects that GPO IOREQ has been dropped, it reads the device status lines and drops the handshake line GPO ADAPTER RESPONSE, thus completing the transfer of a single byte. The dropping of GPO ADAPTER RESPONSE will automatically cause the GPO interface logic to raise GPO IOREQ (5), thus prompting the Host to send it another byte of data. This sequence continues until the complete message has been sent.

Following transmission of the last byte of the message, the Host will raise the status line GPO EOM (6), while putting a dummy byte of data on the data lines. Because the GPO Interrupt Handler checks for special conditions before accepting a data byte, it ignores it and processes the EOM condition.

In EOM processing, the GPO Firmware verifies that both the primary and secondary control units have received exactly the same message, and that the message format is correct. In order to have correct format, a message must contain STX and ETX characters in the correct positions, must not contain any illegal characters, and must be of sufficient length to meet the minimum length requirement of 12 characters (see paragraph 4.1.1).

If an inconsistency is detected DSL6 is raised (see paragraph 2.1.4.6). If the message has been received correctly by both units, the GPO Firmware prepares itself for the next message. It also clears the

internal line GPOABORTENB to prevent the hardware from generating a false abort interrupt. Next, it clears the internal line MSGXFREN and pulses GPOINTACK/ which causes GPO IOREQ to drop ⑦ (MSGXFREN low keeps GPO IOREQ low).

If the message sent by the Host is a type 30 (Invoke Secondary, paragraph 5.1.4) or a type 79 System Checkout of Peripheral Equipment (SCOPE) System Reset, paragraph 5.1.7), the internal line MSGXFREN is kept low, maintaining GPO IOREQ inactive. This is necessary because both messages require immediate processing by the control unit before any other messages may be accepted.

If the message received was not a type 30H or 79H, the received message is placed on an internal queue to await further processing by the control unit firmware, and the secondary is notified via the ICL to do likewise. GPO Firmware will then raise MSGXFREN thereby allowing GPO IOREQ to go active. Upon completion, FDIO will be ready to receive the next message.

2.1.4.3 GPO Abort Operation Signal Sequences. Refer to figure 2-5 for signal sequences.

The GPO Abort operation is performed whenever the transmission of the message in progress needs to be discontinued. The Abort operation could have been caused by a number of reasons. The Host has found a need for an abort or a parity error has been detected, the message has exceeded the maximum message length, the message format has been found to be incorrect or an inconsistency has been detected between the primary and secondary control unit. Independent of its reason, the function of the GPO Abort operation is to clear the message that caused the Abort operation from the system and to prepare the system for the next message. This next message could well be a retransmission of the aborted message, but not necessarily so. The GPO Abort operation is defined as the condition in which the Host drops ADAPTER SELECT during a GPO message transmission prior to dropping GPO EOM ①. GPOABORTENB, which enables the abort detect circuit, is normally set high at the beginning of a message and cleared at the end of a successful message. This avoids the possibility of a transient signal causing a false abort interrupt.

When an abort condition occurs, the interrupt line GPOINT is raised ② and the GPOABORT status bit is set. The interrupt invokes GPO interrupt firmware which recognizes the abort condition by reading the GPOABORT status bit. Abort interrupt firmware clears GPOABORTENB ③ to prevent any further GPO interrupts from occuring. MSGXFREN is cleared to prevent the hardware from raising I/O request again before the abort operation has been fully processed. The aborted message is purged from the buffers, and the secondary is notified via the ICL to do likewise.

Upon completion, MSGXFREN will be raised, which will enable GPO IOREQ ④ to go active providing ADAPTER SELECT is active. At this time, the control unit is ready to receive the next message.

GPO ABORT OPERATION SIGNAL SEQUENCE

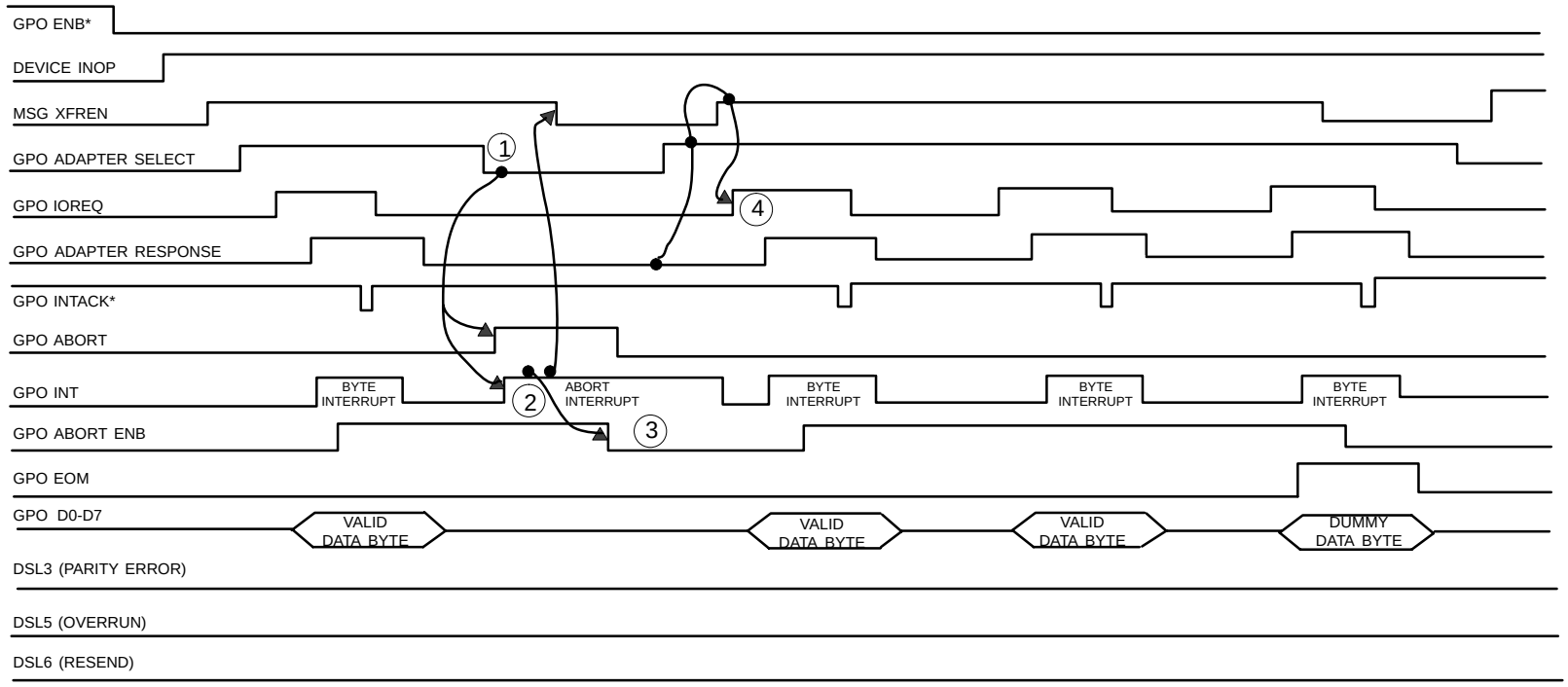


FIGURE 2-5. GPO ABORT SIGNAL SEQUENCE DIAGRAM

2.1.4.4 GPO Parity Error Signal Sequences. Refer to figure 2-6 for signal sequences.

During the transmission of a GPO message, the hardware checks the validity of the data lines through a parity checking mechanism. If a parity error exists, the status bit BADGPOPAR will have been set by the parity detect logic (1). The GPO interrupt firmware tests the status bit, and upon sensing the parity error raises the DSL3 status line to inform the Host of the error condition. Next, GPOINTACK/ is pulsed low to clear GPO IOREQ (2).

The Host responds to DSL3 being set by dropping ADAPTER SELECT (3). Since GPOABORTENB is active, this will initiate the abort sequence as described in paragraph 2.1.4.3, beginning with an abort interrupt. As a result, the current message is cleared from the GPO buffer and the system is ready to receive the next message, which may be a retransmission of the previous message. The GPO abort interrupt handling firmware clears DSL3.

2.1.4.5 GPO Overrun Error Signal Sequences. Refer to figure 2-7 for signal sequences.

During the transmission of a message the GPO Interrupt Handler checks the length of the message against the maximum message length which is 1,712 characters. When the message is about to exceed this maximum with the current data byte, the GPO interrupt handler raises the status line DSL5 to indicate this overrun condition to the Host (1) and pulses GPOINTACK/ low to clear GPO IOREQ. The Host responds to DSL5 being set by dropping ADAPTER SELECT (2).

The Host responds to DSL5 being set by dropping ADAPTER SELECT. Since GPOABORTENB is active, this will initiate the abort sequence as described in paragraph 2.1.4.3, beginning with an abort interrupt. As a result, the current message is cleared from the GPO buffer and the system is ready to receive the next message. The GPO abort interrupt handling firmware clears DSL5.

2.1.4.6 GPO Resend Signal Sequences. Refer to figure 2-8 for signal sequences.

At the end of the message, the Host raises the line GPO EOM (1) and places a dummy byte of data onto the GPO data lines. The GPO Interrupt Handler detects this situation and invokes the GPO Firmware to perform its EOM processing. During this processing the GPO firmware in the primary control unit performs several checks on the received message. When the secondary control unit is available, the primary unit verifies that the secondary has received exactly the same message. This is achieved by comparing a checksum that both units have accumulated during the receive operation. If an inconsistency in the checksum is found, the primary unit raises the status line DSL6 (2) and pulses GPOINTACK/ low to clear GPO IOREQ. The Host responds to DSL6 being set by dropping ADAPTER SELECT (3). Since GPOABORTENB is still active, this will cause an abort interrupt to occur. In this situation, the abort interrupt does not signify a GPO abort condition, but serves to allow the interrupt firmware to tidy up, clear the current message from the GPO buffer, and prepare the system to receive the next message.

If the checksums do compare, then both the primary and secondary unit have received exactly the same message. Next, the GPO Firmware in the primary unit checks the format of the message. The text portion of message, for example, must start with an STX and end with an ETX character. If an inconsistency is found in the format of the message, DSL6 is raised and the Host will abort the message as described in the previous paragraph. The GPO abort interrupt handling firmware clears DSL6.

Following message check and verification, the received message is placed on an internal queue to await further processing by the control unit firmware, and the secondary is notified via the ICL to do likewise. GPO Firmware will then raise MSGXFREN thereby allowing GPO IOREQ to go active. Upon completion, the system will be ready for the next message.

GPO PARITY ERROR SIGNAL SEQUENCE

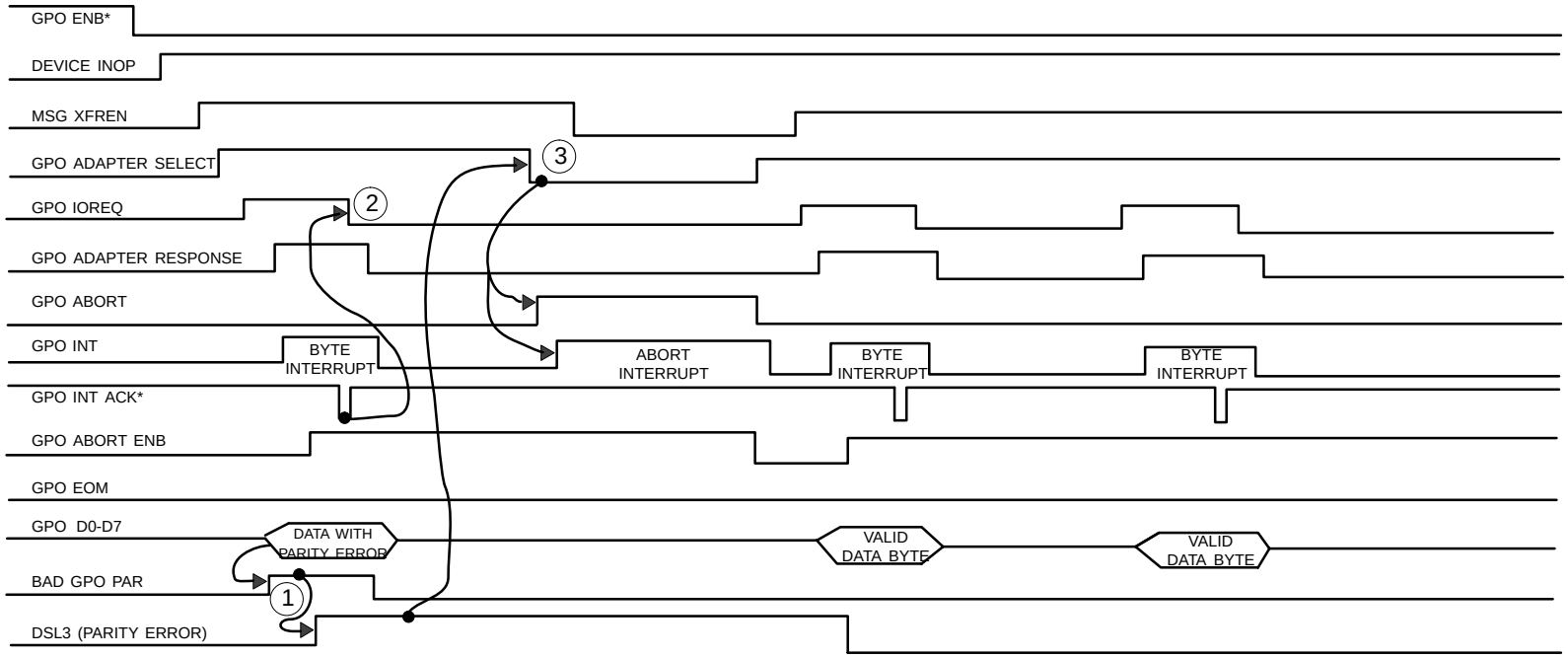


FIGURE 2-6. GPO PARITY ERROR SIGNAL SEQUENCE DIAGRAM

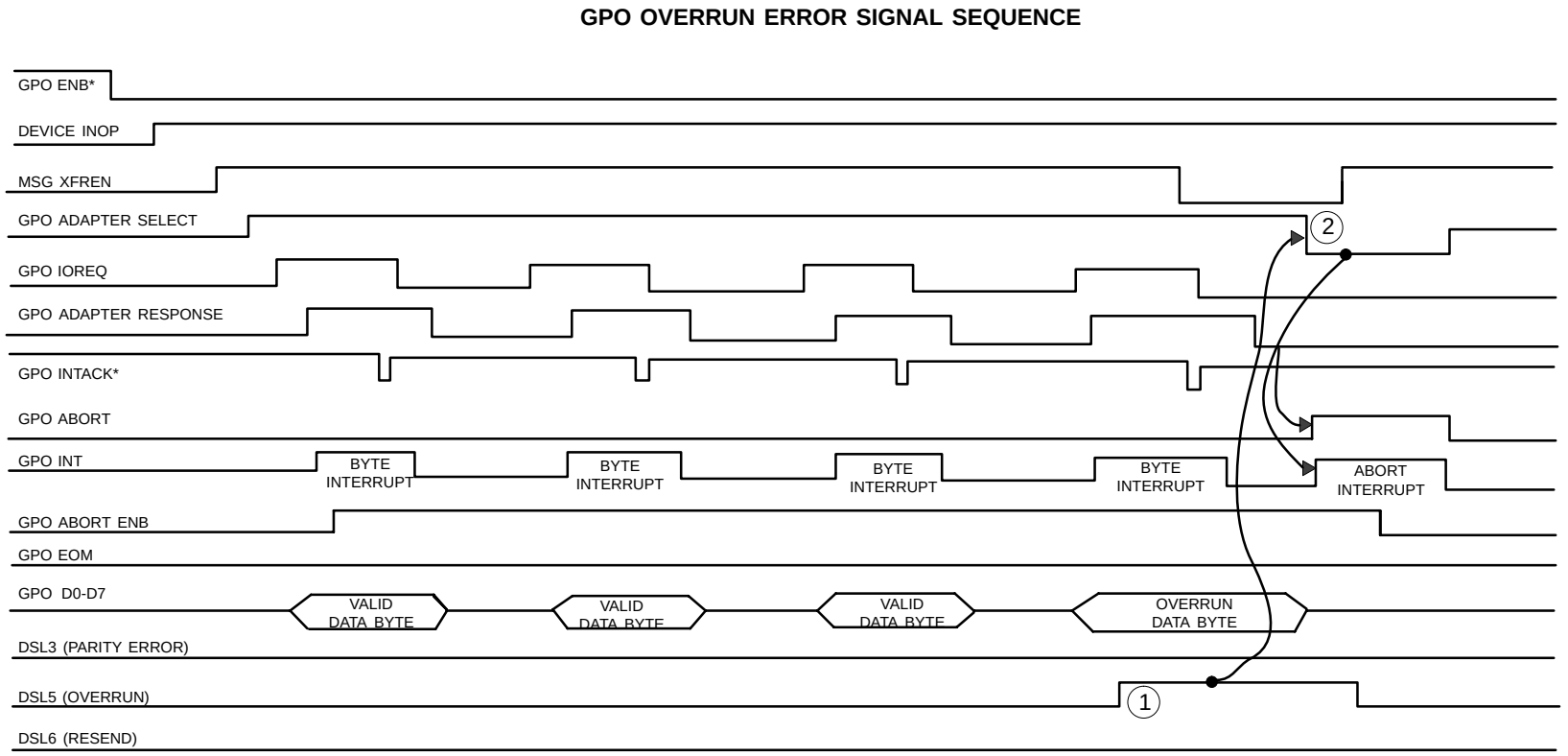


FIGURE 2-7. GPO OVERRUN SIGNAL SEQUENCE DIAGRAM

GPO RESEND SIGNAL SEQUENCE

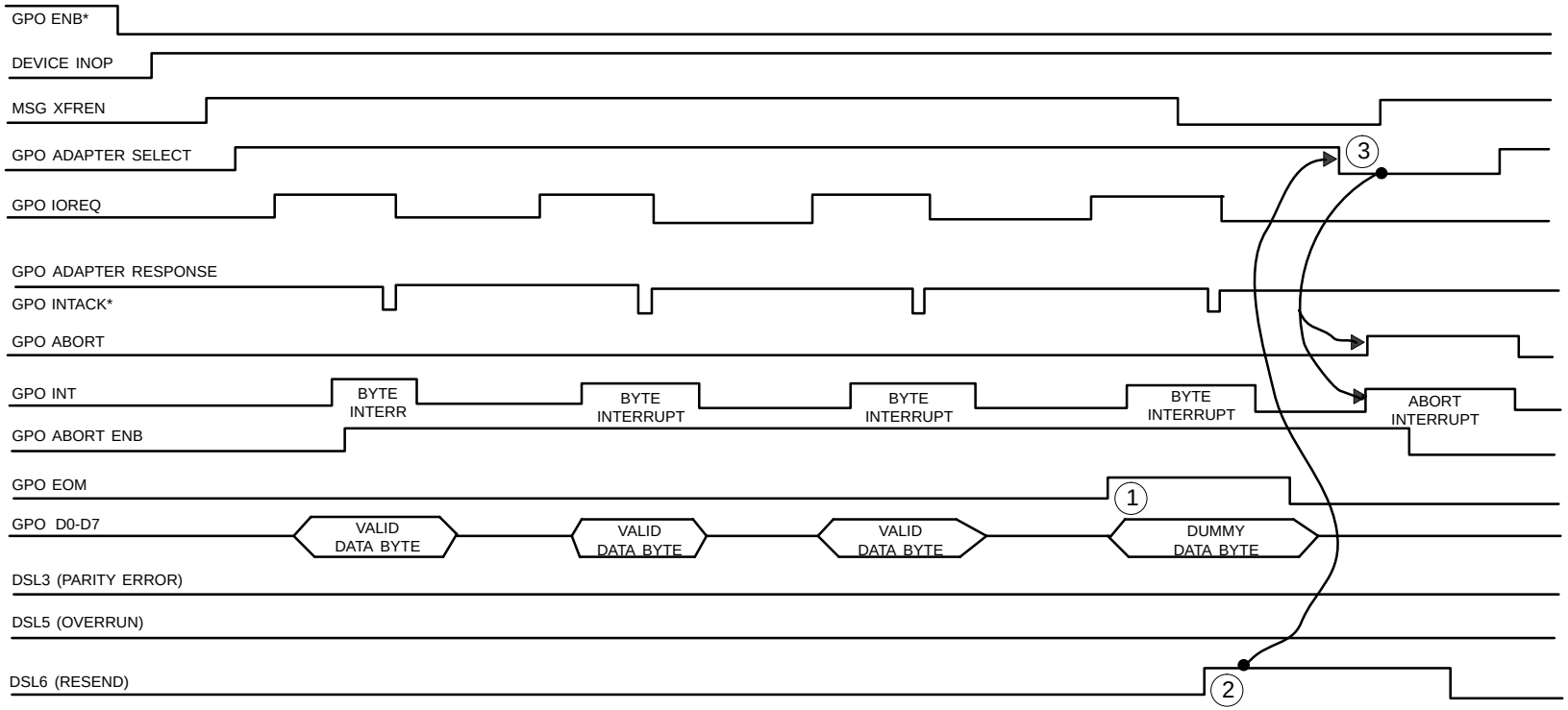


FIGURE 2-8. GPO RESEND SIGNAL SEQUENCE DIAGRAM

2.1.5 Status and Sense Information

2.1.5.1 GPO Unavailable Condition. The FDIO GPO interface can appear unavailable to the Host by enabling (=0) the DEVICE INOPERATIVE interface line. This is done by disabling the signal GPO ENB/ (=1).

As part of the control unit initialization, DEVICE INOPERATIVE will be set inactive (=1) when the primary control unit is ready to receive messages from the Host.

2.1.5.2 GPO Busy Condition. When the CCU or PCU is unable to accept additional information from the Host via the GPO interface, it disables the setting of the interface line GPO IOREQ by disabling (=0) the signal MSGXFREN. This temporarily disables the GPO interface since FDIO will not indicate it is ready for a transmission. When the control unit is again able to receive information from the Host, it enables MSGXFREN, thus allowing GPO IOREQ to become active. A busy condition could arise if there were no more buffers available for additional incoming GPO messages or a control unit switch is in progress.

2.1.5.3 GPO Retransmission Conditions. The following four conditions could invoke a retransmission of the message:

1. Parity error
2. Overrun error
3. Bad checksum
4. Bad message format

2.1.5.3.1 Parity Error. Each character that is received will be checked for parity errors by the hardware. If a parity error is detected, the GPO firmware will raise the status line DSL3. This condition will cause an Abort operation as described under the section GPO Signal Sequences. The Host will retransmit the entire message when the control unit finds a parity error. The number of times a message, reported to contain a parity error, will be retransmitted over the GPO will be determined by the Host.

2.1.5.3.2 Overrun Error. The GPO Firmware checks the length of the received message against the maximum message length. If an overrun error is detected, the status line DSL5 will be raised. This condition will cause an Abort operation as described under paragraph 2.1.4. The Host will determine if a retransmission is applicable.

2.1.5.3.3 Bad Checksum. At the end of each message, the primary control unit will compare its own checksum with that of the secondary control unit. This is done to assure that both units have received exactly the same message. If an inconsistency is found, the status line DSL6 will be raised. Upon sensing DSL6, the Host will prepare to retransmit the entire message, although due to the queue structure of the Host, it may not be the next message transmitted. The number of times a message, reported to generate checksum errors, will be retransmitted over the GPO will be determined by the Host.

2.1.5.3.4 Bad Message Format. The GPO Firmware in the primary control unit performs a format check on the received message. The text field of the message, for example, must start with an STX and end with an ETX character. In addition, the message must have a minimum message length. If an inconsistency is found, the status line DSL6 will be raised. Upon sensing DSL6, the Host will prepare to retransmit the entire message as described in paragraph 2.1.5.3.3. Host will determine if a retransmission is applicable.

2.1.5.4 GPO Time-Out Conditions. There are no time-out restrictions on GPO intercharacter delay.

2.1.5.5 GPO Error Conditions. The GPO Firmware will generate an error message for the System Error Handler during the following conditions:

1. Parity error
2. Overrun error
3. Bad checksum
4. Bad message format

In addition, the GPO Firmware invokes a GPO diagnostics routine each time it processes an abort operation. If a problem is found with the GPO hardware during the diagnostics, an error message is generated for the System Error Handler.

The parity error condition is handled slightly differently from the other error conditions. An error message is only generated if the parity error occurs a second time in the same message.

2.1.6 Resetting the GPO Interface

The GPO interface is reset in the same manner as it was initially set up (see paragraph 2.1.3.1). A reset of the GPO interface occurs to a new primary control unit following a control unit switch.

2.2 GPI INTERFACE

Figure 2-9 shows the GPI interface within the FDIO system.

The CCU and PCU send messages to the GPI adapter at the Host via the GPI interface. Each CCU and PCU consist of two control units, a primary control unit, and a secondary control unit which is configured as a redundant pair. The GPI interface is connected at the FDIO in a daisy-chain fashion from the primary control unit to the secondary, however, only the primary control unit may transmit messages to the Host, since the secondary GPI interface drivers are electronically disabled (see figure 2-2).

2.2.1 General Description

The PCU and CCU control units send messages to the Host in bit parallel, byte serial fashion, over the GPI interface. The GPI interface consists of eight data lines, a parity line, handshake lines, and control lines. Table 2-3 provides a list and description of the physical interface lines associated with the GPI interface.

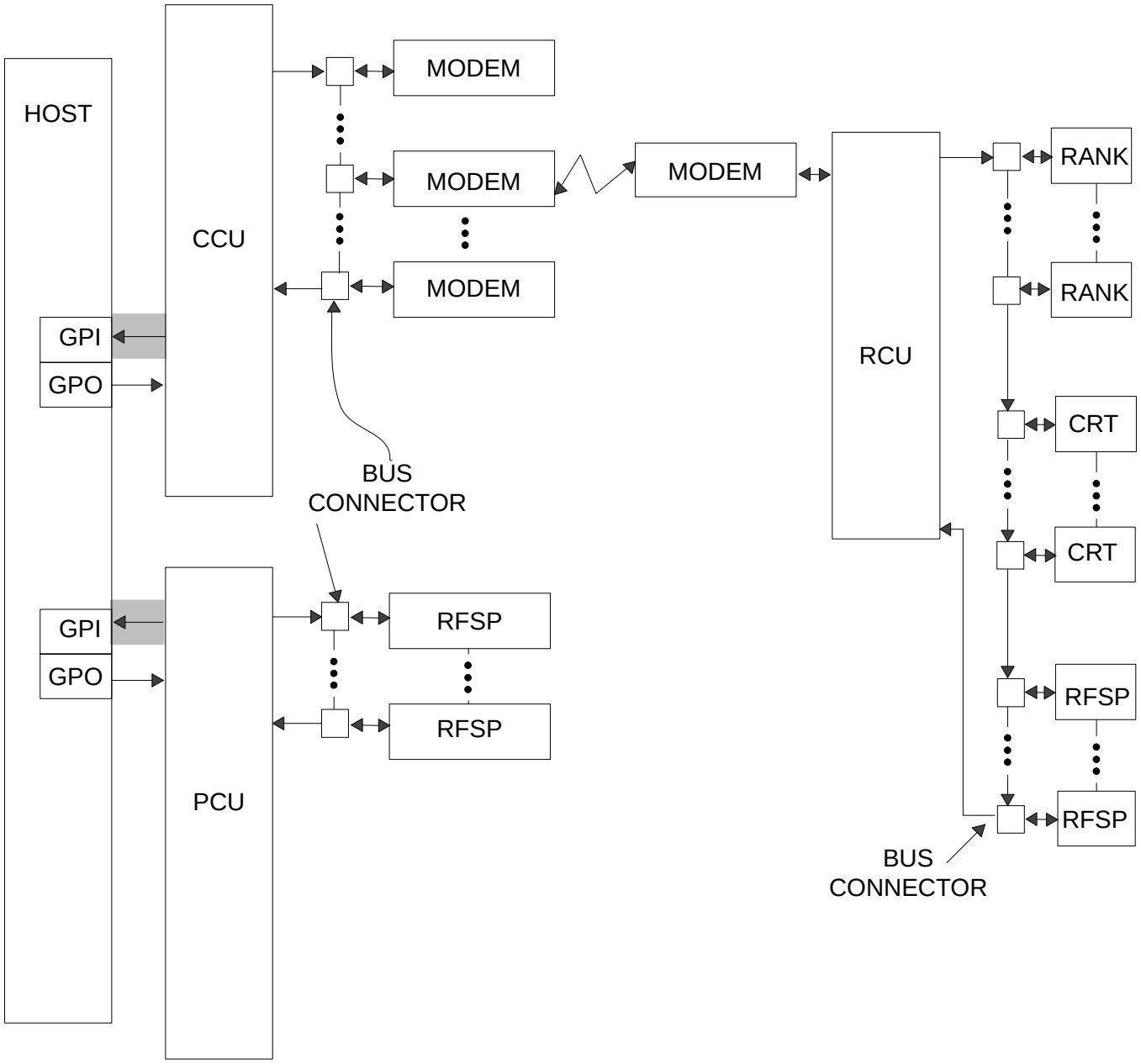


FIGURE 2-9. GPI INTERFACE

TABLE 2-3. GPI INTERFACE SIGNAL DEFINITION

Interface Line	Function [note 1]
DATA LINES	
GPI data 0 (D0)	most significant data bit
GPI data 1 (D1)	
GPI data 2 (D2)	
GPI data 2 (D2)	
GPI data 3 (D3)	[data is in 8-bit IBM format]
GPI data 4 (D4)	
GPI data 5 (D5)	
GPI data 6 (D6)	
GPI data 7 (D7)	least significant data bit
GPI parity	parity bit added to data bits
HANDSHAKE LINES [note 2]	
GPI I/O Request	request by CCU/PCU to send a character
GPI Adapter Response	indicates the Host has sampled the data, parity and EOM lines
GPI EOM	EOM
DEVICE CONTROL LINES [note 2]	
Device Control Line 1	Host is ready to accept (DCL1)
Device Control Line 3	Host received parity error (DCL3)
Device Control Line 4	force control unit switch [note 3] (DCL4)

NOTES

1. All interface signals are active when they are high.
2. These lines are referred to in the PAMRI manual as control lines.
3. A control unit switch occurs if DCL1, DCL3, and DCL4 are all active at the same time.

2.2.1.1 GPI Block Diagram. The GPI interface consists of the following functional building blocks as shown in figure 2-10:

a. Transmit Signal Buffers — This section contains the circuitry that buffers and transmits the GPI data and handshake signals to the Host GPI adapter.

b. Parity Check Logic — This section sets the GPI parity bit to the correct parity according to the data byte being transmitted.

c. Parallel Peripheral Interface — This circuit consists of a PPI chip which presents the GPI data byte to the transmit buffers. In addition, it controls the handshake sequencing necessary

to interface with the Host GPI adapter, as well as generate the GPI hardware interrupt that is sent to the PIC.

d. Receive Signal Buffers — This section contains the circuitry that receives and buffers the control and handshake lines.

2.2.2 Device Addressing

2.2.2.1 GPI PPI. The GPI PPI contains three 8-bit I/O ports, A, B, and C which are utilized by the GPI interface to output the GPI data character as well as control the GPI interface logic. The GPI PPI is a memory mapped device with the address assignments shown in table 2-4.

TABLE 2-4. GPI PPI ADDRESSING

Memory Address	Function
F800	PORT A — output: 8-bit GPI data character
F801	PORT B — input: GPI control and status lines
F802	PORT C — output: GPI handshake lines
F803	CONTROL REGISTER — output

2.2.2.2 PIC. The PIC receives the GPI interrupt generated by the GPI handshake logic. It is addressed as an I/O device and is assigned addresses E0 and E1 hex. See appendix A for complete information regarding PIC operation.

2.2.3 GPI Interface Control Commands

2.2.3.1 GPI Interface Setup Commands. Before GPI operation can commence, the GPI PPI controller must be initialized to place the three 8-bit ports into the correct operating mode. Port A and the upper four bits of port C operate in the automatic handshake mode (mode 1 of the 8255 PPI controller), and will generate the GPI interrupt at the appropriate time. The setup sequence must enable this interrupt mechanism within the GPI PPI. In addition, the PIC must be set up to recognize the GPI interrupts.

2.2.3.1.1 GPI PPI Initialization. The GPI PPI setup requirements are as follows:

a. Port A programmed to output mode with auto handshake

b. Port B programmed to input mode

c. Port C (upper 4 bits) programmed to output with auto handshake

d. Port C (lower 4 bits) programmed to output mode

e. EOM line, set inactive

f. GPI handshake lines initialized

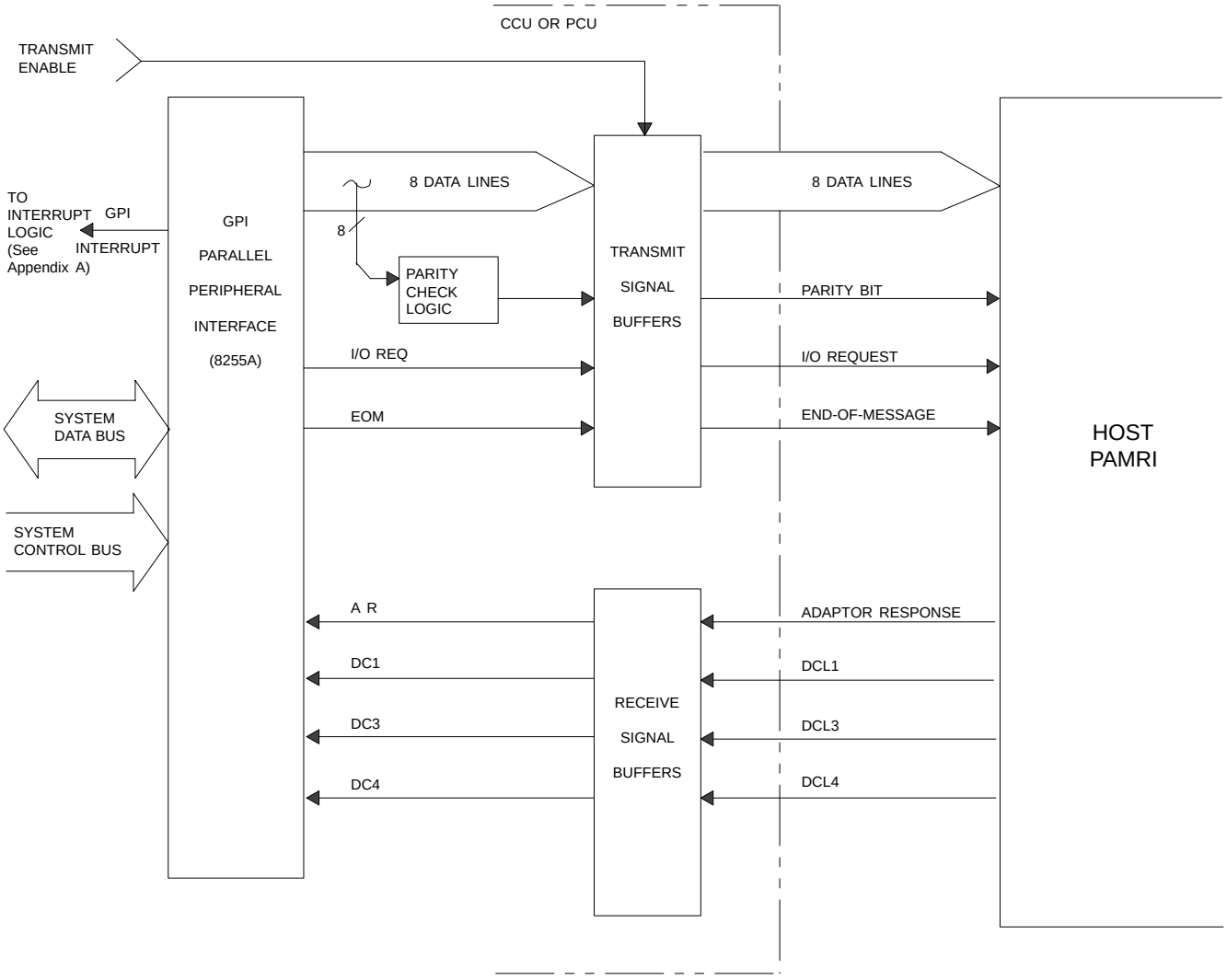


FIGURE 2-10. GPI BLOCK DIAGRAM

The GPI PPI setup will be performed by writing to its control register and by initializing the output bits as follows:

Command Operation	Command Memory Address	Command Contents (binary)	Command Description
OUTPUT	F803	10100010	Set port A to output mode Set port B to input mode Set upper port C to output Set lower port C to output
OUTPUT	F800	00000000	Initialize port A: clear the GPI data byte
OUTPUT	F802	00100000	Initialize port C: GPI handshake logic
OUTPUT	F803	00000111	Set to enable GPI interrupt

2.2.3.1.2 PIC Initialization. The PIC consists of an 8259A LSI device. The PIC setup is described in appendix A.3.

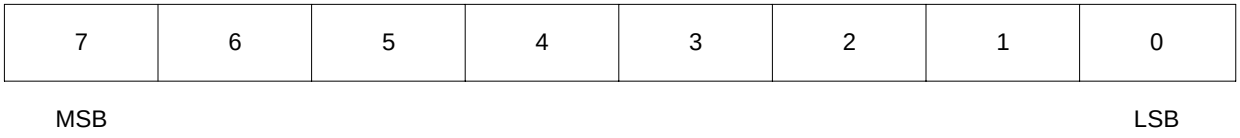
2.2.3.2 GPI Operational Commands. GPI operational commands involve the setting of control bits and the reading of status bits at certain points within the GPI transmit operation. In addition, the PIC must be instructed to update its internal interrupt status following each GPI interrupt.

2.2.3.2.1 GPI Data and Control Bits. The GPI hardware circuitry is controlled by the GPI firmware, resident in the control unit (CCU or PCU), via the GPI PPI controller. Port A is configured as as output, providing for the eight GPI data bits. Port C is configured for five output control bits (not to be confused with the DCL lines), two handshake bits and an interrupt bit.

The 8-bit GPI data character is output by writing to port A of the GPI PPI, memory address F800 (hex):

Bit	Description
0-7	GPID0-GPID7 — 8-bits of GPI data.

The following control bits are available by writing an 8-bit control word to port C of the GPI PPI, memory address F802 (hex):



Bit	Description
0	EVEN PARITY — When inactive (low), this signal sets the parity for the GPI character to odd.
1	WAIT DCL1 — When active (high), this signal enables the circuit that tests for DCL1 going inactive.
2	CLR GPIINT/ — When active (low), this signal clears the GPI interrupt request signal.
3	GPIINTREQ — This signal invokes a hardware interrupt and is generated automatically by the GPI PPI when a character has been sent.
4	GPIEM — When active (high), this signal raises the GPI EOM interface line.
5	GPIENB — When active (high), this signal enables the GPI transmit buffers of the primary control unit.
6	ACK/ — This is an automatic handshake signal and receives GPI ADAPTER RESPONSE.
7	OBF/ — This is an automatic handshake signal and activates GPI IOREQ.

2.2.3.2.2 GPI Status Bits. Port B of the GPI PPI is configured as an input port and allows for the reading of eight GPI status bits (not to be confused with the DSL). This is accomplished by reading memory address F801 (hex).

Bit	Description
0	GPIPAR — This bit is a copy of the parity bit output of the parity generator that is sent out over the GPI interface.
1	ICL INT/ — This bit is used by the ICL interrupt handler.
2	CKFORPAR — This bit is set when DCL1 drops low.
3	GPIABORT — This bit is set whenever DCL1 drops low causing a GPI abort condition.
4	GPIDCL5 — This bit is a copy of DCL5 (not used).
5	GPIDCL4 — This bit is a copy of DCL4.
6	GPIDCL3 — This bit is a copy of DCL3.
7	GPIDCL1 — This bit is a copy of DCL1.

2.2.3.2.3 PIC Operational Control. The PIC must be informed when the GPI interrupt service routine is being exited. This will reset the 8259A PIC internal-in-service register and enable other interrupts. This will be accomplished by executing the following command:

Command	Address	Data	Command Description
OUTPUT	00EO	20 (hex)	Perform end-of-interrupt operation

2.2.4 GPI Write Signal Sequences

The following three sections describe the GPI signal sequences:

1. 2.2.4.1 GPI Initialization Signal Sequences
2. 2.2.4.2 GPI Normal Operation Signal Sequences
3. 2.2.4.3 GPI Resend Signal Sequences

Figures 2-11 and 2-12 are signal sequence diagrams and provide additional information relative to the different GPI signals and operations. They do not show absolute timing relationships and should not be used for that purpose. The numbers in circles correspond to the descriptions referenced in the text.

2.2.4.1 GPI Initialization Signal Sequences. The initialization of the GPI hardware proceeds in two stages. The first part occurs at power-up or reset, when the operating mode of the GPI PPI controller is established, the handshake logic is reset and the transmit buffers are disabled by dropping (=0) GPIENB.

The second part of the GPI Initialization is performed at a later time when it is known to the control unit whether it will operate as a primary or secondary unit. If the control unit is a primary unit, the GPI transmit buffers are enabled by activating GPIENB (high). In addition, GPI interrupts are disabled by setting CLR GPIINT/ low to avoid false interrupts during the initialization period. If the control unit is a secondary unit, no hardware is initialized. The only function of the secondary GPI Firmware is to accept release message commands from the primary control unit.

2.2.4.2 GPI Normal Operation Signal Sequences. Refer to figure 2-11 for signal sequences.

At the end of the initialization phase, the GPI Firmware activates (=1) GPIENB ①, at which time it is ready to send messages to the Host. When the GPI Firmware receives a message to transmit, it starts monitoring the status line DCL1. As soon as the Host raises this control line ②, the GPI Firmware puts the first byte of the message onto the data lines GPI DATA0-GPI DATA7 and enables GPI interrupts by raising CLR GPIINT/ (=1). The GPI PPI raises the handshake line GPI IOREQ to indicate to the Host that a byte is pending on the data lines. The Host reads this byte and responds by raising GPI ADAPTER RESPONSE to indicate that it has received the byte. The hardware then clears GPI IOREQ which causes the Host to drop GPI ADAPTER RESPONSE. As a result of GPI ADAPTER RESPONSE dropping, the GPI interrupt line GPIINT is set ③ which invokes the GPI interrupt handler.

The GPI Interrupt Handler will put the next byte on the data lines and the sequence starts all over again. In this manner, the entire message will be sent to the Host, one byte at a time. As each byte is sent to the Host, the internal byte count is decremented. When this count reaches zero, the entire message will have been sent.

GPI NORMAL OPERATION SIGNAL SEQUENCE

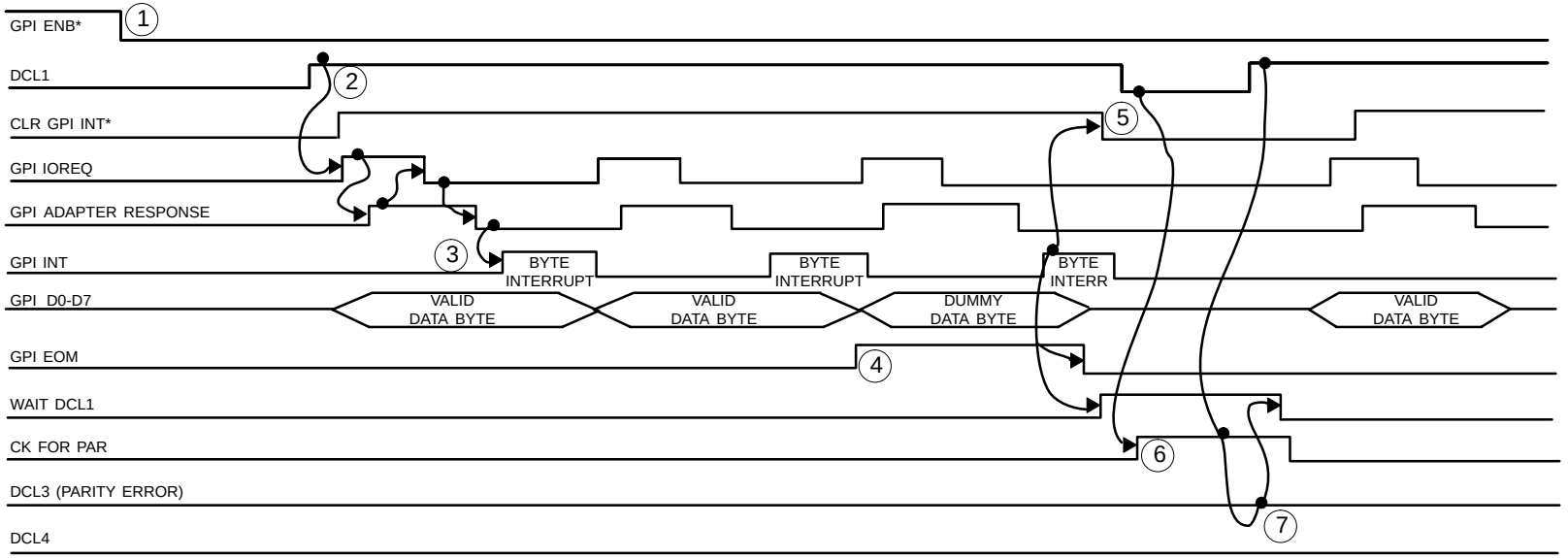


FIGURE 2-11. NORMAL GPI SIGNAL SEQUENCE DIAGRAM

GPI RESEND OPERATION SIGNAL SEQUENCE

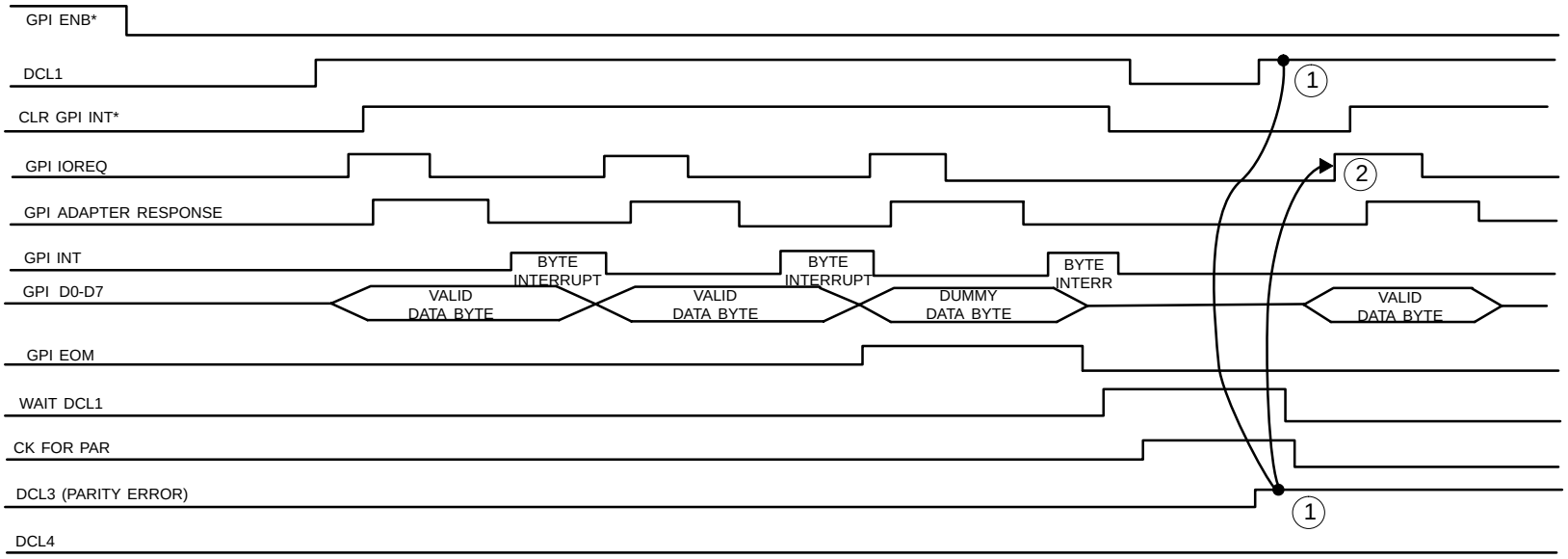


FIGURE 2-12. GPI RESEND SIGNAL SEQUENCE DIAGRAM

At the end of the message, the GPI Interrupt Handler will raise the interface line GPI EOM while putting a dummy byte on the data lines ④. After the Host drops GPI ADAPTER RESPONSE, the hardware will generate the last interrupt of the message transfer. The GPI Interrupt Handler uses this interrupt to clear GPI EOM and to disable further GPI interrupts by activating (=0) CLR GPIINT/ ⑤. In addition, it enables a circuit which detects when the Host drops DCL1 by setting the internal line WAIT DLC1.

The Host indicates the completion of the GPI read operation by dropping DCL1. If the message was received correctly, DCL3 will remain low when DCL1 is raised at the start of the next GPI message transfer. If the message was received with an error, the Host will raise DCL3 and DCL1 at the same time.

The hardware will detect the high to low transition of DCL1 and will set status bit CK FOR PAR ⑥. By monitoring CK FOR PAR, as well as DCL1, the correct time for monitoring the DCL3 line from the Host can be determined (i.e., when DCL1 goes high again).

When GPI firmware detects DCL1 going high following it being low, it reads the status line DCL3 ⑦. If the status line DCL3 is high, it will perform the resend procedure (see paragraph 2.2.4.3). Otherwise, it releases the message from its queue for processing, clears WAIT DCL1, and notifies the secondary control unit via ICL of the successful transmission. The secondary control unit maintains the same queue and will also release the message from its queue. The control unit is now ready to send the next message.

2.2.4.3 GPI Resend Signal Sequences. Refer to figure 2-12 for signal sequences.

At the end of the message, the GPI Firmware will wait for the status of the message from the Host. If an error has been found, the Host will raise DCL1 and DCL3 together ①, indicating that the message is to be resent.

When the GPI firmware detects this resend condition, it first calls the GPI diagnostic to test the GPI hardware. If a problem with the hardware is found, an appropriate system error is posted to the front panel. The original message is then retransmitted following the normal operating sequence of events outlined above ②. It is up to the Host to perform a control unit switch if the failure is within FDIO.

2.2.5 Status and Sense Information

2.2.5.1 GPI Unavailable Condition. The Host PAMRI indicates its availability to perform input from the FDIO system by raising DCL1. When DCL1 is inactive (low), FDIO may not send information to the Host via the GPI interface.

2.2.5.2 GPI Busy Conditions. When the CCU or PCU is not ready to transmit information to the Host via the GPI interface, it does not activate the GPI IOREQ handshake signal. When there is information to send, an 8-bit data character is output on the eight GPI data lines and GPI IOREQ is activated. This condition arises if there is no GPI data to be transmitted, or a control unit switch is being performed.

2.2.5.3 GPI Retransmission Conditions. When a message has been received in error, the Host may request a retransmission by raising the status line DCL3. The Host determines how many times a retransmission will be requested. The GPI Firmware in the control unit will keep the current message stored in its buffers until it has positive acknowledgement that the message has been received correctly. The positive acknowledgement consists of the absence of the status line DCL3 when the status line DCL1 is raised again.

Possible causes of a retransmission could be, for example, parity errors detected by the Host, or a buffer overflow in the Host caused by an overrun error.

2.2.5.4 GPI Time-Out Conditions. There are no time-out restrictions.

2.2.5.5 GPI Error Conditions. The GPI Firmware generates an error message for the System Error Handler when it detects that Host has requested a retransmission of the same message for the second time. In addition, the GPI Firmware invokes a GPI diagnostic routine each time it processes a retransmission operation. If a problem is found with the GPI hardware during the diagnostic, an error message will be generated for the System Error Handler.

2.2.6 Resetting the GPI Interface

The GPI interface is reset in the same manner as it was initially set up (see paragraph 2.2.3.1). A reset of the GPI interface occurs to a new primary control unit following a control unit switch.

2.3 PERIPHERAL DEVICE INTERFACE

Figure 2-13 shows the peripheral device interface within the FDIO system.

2.3.1 General Description

The peripheral device interface is the communications link whereby messages originating within the Host or the FDIO system are displayed on CRTs and RFSPs, and RANK input messages are entered into the system to ultimately be sent to the Host or used internally.

Each peripheral device interface consists of a BC located at a PCU or an RCU, an interface cable, and a peripheral device. The PCU can communicate with up to 29 peripheral devices consisting of 28 RFSPs and a maintenance channel. The RCU can communicate with up to 21 peripheral devices, consisting of up to 10 RFSPs, 5 RANKs, 5 CRTs, and a maintenance channel. An interface cable of up to 4000 feet in length links the BC with the peripheral device. Table 2-5 provides a description of the interface cable.

TABLE 2-5. PERIPHERAL DEVICE INTERFACE SIGNAL DEFINITION

The interface connector is a DB-25 with the following pins assigned to the RS-422 functions.

PIN	FUNCTION	DESCRIPTION
15	RX-	Data to printer (-)
17	RX+	Data to printer (+)
19	TX-	Data from printer (-)
25	TX+	Data from printer (+)
1	FGND	Frame ground
7	SGND	Signal ground

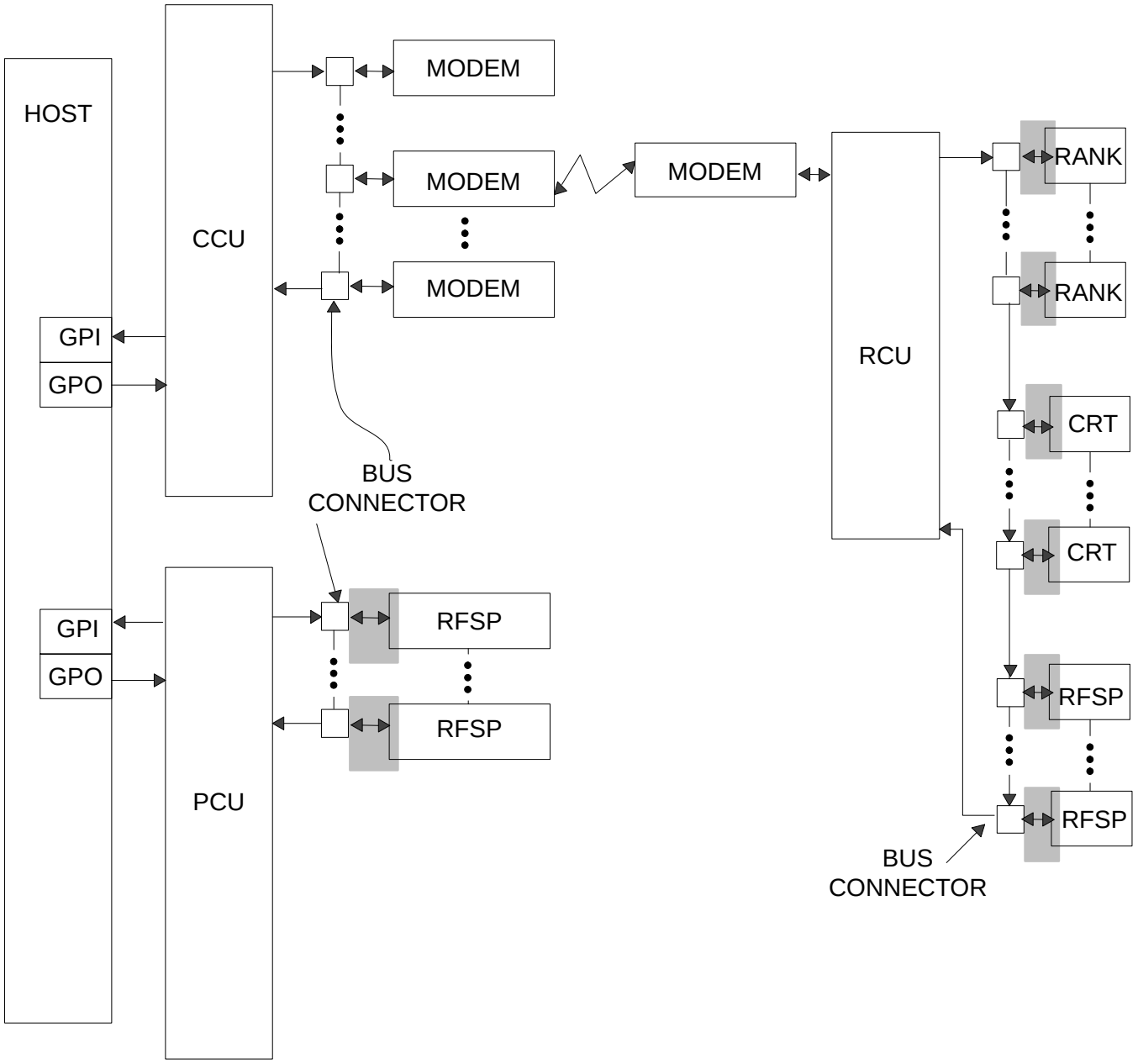


FIGURE 2-13. PERIPHERAL DEVICE INTERFACE

The communication link consists of a 2400 baud asynchronous serial channel utilizing the RS-422 interface standard.

The peripheral device interface consists of the following building blocks as indicated in figure 2-14:

a. Asynchronous Communications Controller — The asynchronous serial communications controller is an integral part of the 8031 microprocessor and provides the interface between the parallel processor of the BC and the serial peripheral device (RFSP, CRT, or RANK). It performs the parallel to serial and the serial to parallel data conversion functions. Both the receive and transmit operations are performed on a character basis using interrupts.

b. Baud Rate Generator — The asynchronous communications controller requires a baud clock to establish the communications frequency of the asynchronous link. This function is performed by a baud rate generator and is also internal to the 8031 microprocessor.

c. Serial Interface — This circuit provides the appropriate RS-422 drivers and receivers for each of the connected asynchronous peripheral devices.

2.3.2 Device Addressing

Table 2-6 gives the asynchronous serial communications controller addresses.

TABLE 2-6. ASYNCHRONOUS SERIAL COMMUNICATIONS CONTROLLER (8031)

I/O Address	Function
0098	SCON — Serial Port Control Register
0099	SBUF — Serial Port Input/Output Buffer

Table 2-7 gives the baud rate generator addresses.

TABLE 2-7. BAUD RATE GENERATOR (8031)

I/O Address	Function
89	TMOD — Timer/Counter Mode Control Register
8D	TH1 — Baud Rate Constant Register

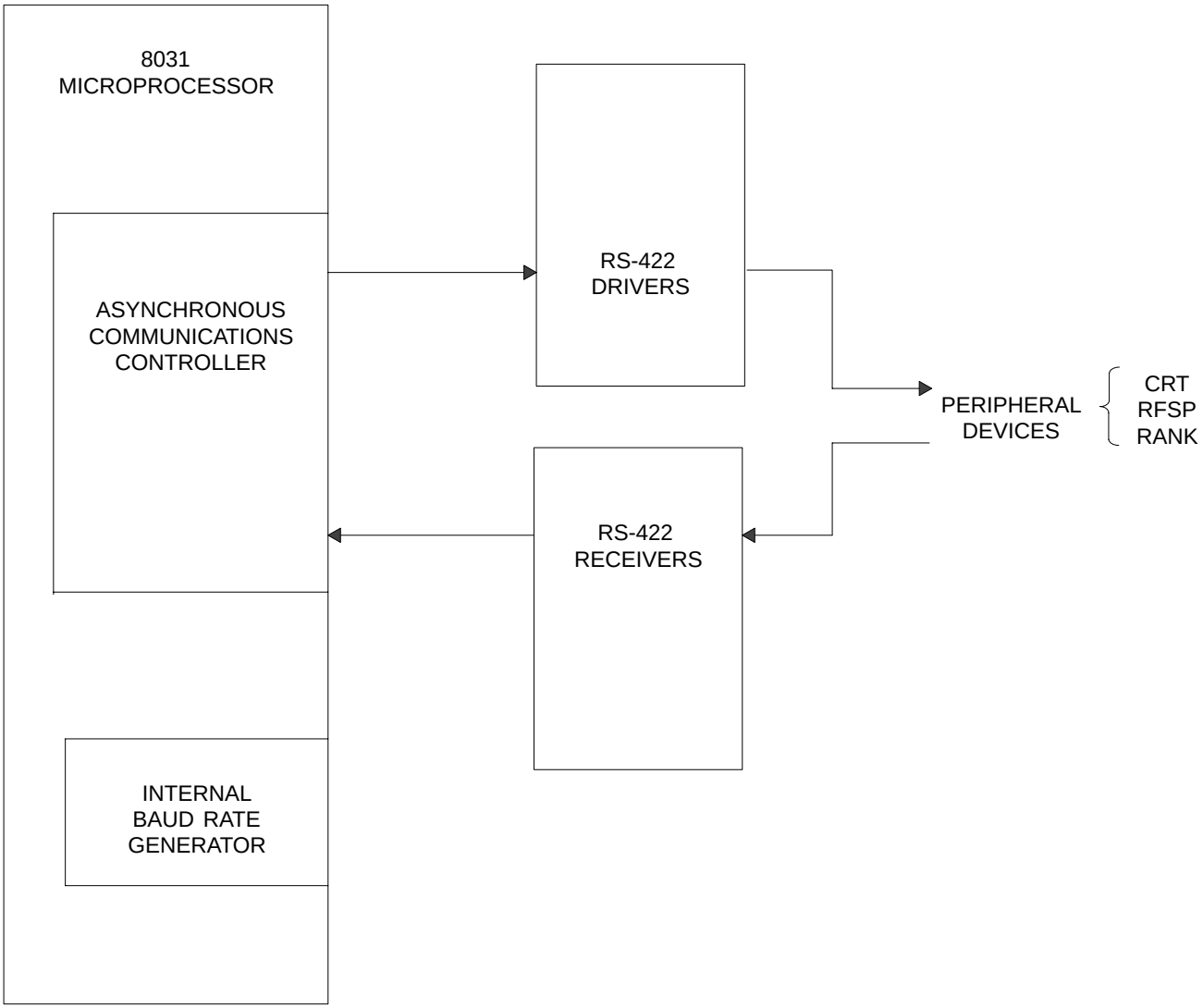


FIGURE 2-14. PERIPHERAL DEVICE INTERFACE BLOCK DIAGRAM

2.3.3 Interface Control Commands

2.3.3.1 Asynchronous Communications Controller Setup Commands. The asynchronous serial communications controller is incorporated within the 8031 processor LSI device and is initialized with the following parameters in order to communicate with the serial peripheral devices:

a. Operation to be asynchronous mode 2

b. 11 bits per character transmitted or received:

1. 1 start bit (0),

2. 8 data bits,

3. 1 parity bit, and

4. 1 stop bit (1).

c. Enable transmit and receive interrupts

d. Enable serial communications circuitry

In order to accomplish the above initialization of the communications interface, the following sequence of commands will be issued:

Command Operation	Command Address (hex)	Command Contents (binary)	Command Description
OUTPUT	98 (SCON)	11010000	8-bit data, 1-bit parity, 1 stop bit, enable rcv, xmt interrupts, enable the receiver circuit

2.3.3.2 Baud Rate Generator Setup Commands. The baud rate generator is incorporated within the 8031 processor LSI device and is initialized with the following parameters to generate a 2400 baud communications clock:

Command Operation	Command Address (hex)	Command Contents (hex)	Command Description
OUTPUT	89 (TMOD)	21	Set the timer mode for baud rate generation
OUTPUT	8D (TH1)	F4	Set up count value for 2400 baud

2.3.4 Signal Sequences

The peripheral device interface provides the hardware mechanism for sending FDIO messages and control sequences to the peripheral devices (i.e., RFSPs, CRTs, and RANKs) and for receiving RANK input messages and status information from these devices. Input messages originating at a peripheral device will be routed and decoded in the BC for transmission to the CCU or PCU.

2.3.5 Output Message Sequencing (Write Operation)

The BC receives the messages from the control unit via the LAN and places them in a circular buffer located in Random Access Memory (RAM) (see FDIO-51G4 for details). This buffer is first-in-first-out, in that the BC handles the messages in the chronological sequence they are received.

The peripheral output operation utilizes interrupt processing to oversee the character by character transmission of the message. The first character of the message is read from the circular buffer and sent to the asynchronous communications controller by performing an output to SBUF (internal memory location 99 hex). Odd parity is calculated on the data byte and the communications controllers parity transmit bit (TB8) is set accordingly. The communications controller converts the 8-bit data and parity bit into a serial bit stream and begins a bit by bit transmission of the nine bits over the serial interface to the peripheral device. The communications controller automatically adds a start and a stop bit the the transmission for a total of 11 bits. When the last bit has been sent, a hardware interrupt is generated which informs BC firmware that the character has been sent out and the communications controller is ready for another character. The next character of the message is obtained from the circular buffer and sent to the communications controller where it is serialized and sent to the peripheral device. This continues in a like manner until the last character has been sent. Interface protocol (see appendix B.3.1) requires that all messages sent to the peripheral device end with an ETX (03 hex) character. This signals the peripheral device that the end of the message has been received and initiates a response sequence.

Upon sending the ETX termination character, the BC initializes an internal timer and begins looking for the correct response sequence. Depending on the content of the message sent out, the BC expects a particular response from the peripheral device (see paragraph 2.3.7).

If the BC fails to receive a correct response, or the internal time-out occurs, a failure condition is noted, the BC attempts to obtain the peripheral status byte (paragraph 2.3.8) and appropriate error handling is invoked. See paragraph 2.3.12 on error conditions for further information.

2.3.6 Input Message Sequencing (Read Operation)

Characters are received from the peripheral device in serial form and are converted to a 9-bit parallel byte (8 bits of data plus a parity bit) by the asynchronous serial communications controller within the BC. When a complete character has been received and converted, a hardware interrupt is generated. Interrupt handling firmware will obtain the character from the communications controller by performing an input from SBUF (internal memory location 99 hex) and check it for correct parity. Characters with correct parity are decoded and acted upon accordingly.

If a character from a RANK is received with a parity error, the character is changed to the special RANK parity symbol (see appendix B.1.2.1) before being transmitted over the LAN to the RCU for processing. If the parity error is associated with a response character from a peripheral device, the response is ignored and an internal time-out occurs. The BC will then try to obtain the peripheral status byte (see paragraph 2.3.8) in an attempt to determine what is wrong with the peripheral device. The control unit (RCU or PCU) will be notified as to the exact nature of the peripheral failure (if any). The BC will not issue the Text Acknowledge message thereby causing the control unit to time-out and either reroute the message to a backup peripheral device or perform appropriate error processing.

2.3.7 Response Sequence

The peripheral device provides the BC with a positive indication that it has received and processed the message by subscribing to a strict interface protocol (appendix B.3 describes the protocol characters

in detail). The protocol requires the peripheral device to respond to all messages received from the BC.

In addition to receiving the correct response sequence from the peripheral device, the BC must receive the response within an appropriate amount of elapsed time. If the response is not received within this time period, an internal time-out will occur and an error condition will exist.

The following paragraphs list the different categories of output messages, together with the appropriate response and maximum time-out values. The maximum time-out values indicate the allowable elapsed time from one response character to the sucessive one.

2.3.7.1 Print Messages. The peripheral device will send the following response sequence to the BC upon sensing the ETX character of an output printable message:

X-OFF	3.0 seconds
{print/display the text}	
ACK/NAK [note 1]	see note 2 for RFSP 0.9 seconds for CRT
X-ON	0.01 seconds

NOTES

1. If the peripheral device receives the message correctly and is able to successfully print or display the message, it will return an ACK. If it did not receive the message correctly, or an error condition exists that prohibits the message from being printed or displayed, it will return a NAK.

2. The time allowed for the RFSP to respond with the ACK/NAK depends on the number of characters in the message being printed. The time-out is calculated using a conservative 100 milliseconds (MSec) per character (10 characters per second), yielding approximately 170 seconds for the maximum length message of 1,712 characters.

Typical operational messages falling into this category are text messages to be printed on an RFSP or displayed on a CRT.

2.3.7.2 RANK Output Messages. The RANK will send the following response sequence to the BC upon sensing the ETX character of a Message Waiting Light (MWL) ON/OFF sequence:

X-OFF	3.0 seconds
{turn MWL on or OFF}	
ACK/NAK [note]	0.9 seconds
X-ON	0.01 seconds

NOTE

If the RANK receives the message correctly and is able to successfully access the MWL, it will return an ACK. If it did not receive the message correctly, or an error condition exists that prohibits the operation from being performed, it will return a NAK.

2.3.7.3 Request Peripheral Status Byte. The peripheral device will send the following sequence to the BC upon sensing the ETX character following a request for the peripheral status byte (see paragraph 2.3.8):

Response Sequence	Maximum Response Time
X-OFF	3.0 seconds
ACK/NAK [note 1]	0.9 seconds
Status Byte [note 2]	0.01 seconds
X-ON	0.01 seconds

NOTES

1. If the peripheral device receives the request for status message correctly and is able to respond with a correct status byte, it will return an ACK. An ACK is the correct response, even if the returned status byte indicates an error condition exists, assuming the peripheral device is able to correctly return the status byte. If the request for status message is received with a parity error, or the status byte cannot be successfully returned, the peripheral device will return a NAK.

2. If a NAK is returned, indicating some sort of error condition, the status byte may or may not accompany the response.

2.3.7.4 BC Initiated Diagnostic. The peripheral device will not send an X-OFF character following receipt of the ETX, but will immediately perform the requested diagnostic. If successful, it will respond with an X-ON character to the BC within 10 seconds. If unsuccessful, the peripheral device will not respond at all.

2.3.8 Peripheral Status Byte

An internal 8-bit status byte is maintained by the peripheral device. This status byte is returned to the BC when the BC sends a request for status message (ESC [x) to the peripheral device. The peripheral device will respond with a single byte of status as follows:

D7	D6	D5	D4	D3	D2	D1	D0

MSB LSB

Bit		Definition		Default State
D7	=	Not Used		0
D6	=	Device Fault		0
D5	=	Out of Paper	[note 1]	0
D4	=	Character Parity Error		0
D3	=	Online	[note 2]	1
D2	=	Device Code	[note 3]	—
D1	=	Device Code	[note 3]	—
D0	=	Device Code	[note 3]	—

NOTES

1. This bit is valid for an RFSP only and is zero for a CRT and RANK.
2. This bit is valid for an RFSP only and is one for a CRT and RANK.
3. The default state depends on the type of peripheral device connected.

2.3.8.1 Device Fault. If the peripheral devices internal diagnostics detect a failure, the device fault bit (D6) of the peripheral status byte will be set (=1). Some of the faults are as follows:

a. Unsuccessful flight strip load

b. Print head jam

c. RAM or Read Only Memory (ROM) Cyclical Redundancy Check (CRC) error

The device fault status bit is reset to its default state only when the fault condition no longer exists.

2.3.8.2 Out of Paper. If an RFSP detects an out of paper condition, the out of paper bit (D5) of the printer status byte will be set (=1). This bit shall be reset when the out of paper condition no longer exists.

2.3.8.3 Parity. The peripheral device checks each incoming character for odd parity. Upon detection of a character parity error, the parity error bit (D4) of the peripheral status byte will be set (=1) and the special parity error character similar to a photographic negative of a question mark  will be printed instead of the character (for an RFSP or CRT). If the parity error is detected as part of a control (escape) sequence, the peripheral device will ignore the escape sequence, print the special parity error character in lieu of the control sequence, and continue printing the remainder of the message. The peripheral device will also respond by sending a NAK to the BC (see paragraph 2.3.7 and appendix B.3). The parity status bit is reset automatically as a result of sending the peripheral status byte to the BC.

2.3.8.4 Online. The online bit (D3) of the peripheral status byte will be set (=1) whenever the RFSP is in an online state. This bit shall be reset when the printer is no longer in the online state.

2.3.8.5 Device Code. The device code bits (D2-D0) are different for each peripheral device and are defined as follows:

D2	D1	D0	Peripheral Device
0	0	0	ILLEGAL
0	0	1	RANK
0	1	0	RFSP (FA 10095/2 and FA 10095/14)
0	1	1	CRT
1	0	0	MODEM
1	0	1	Reserved
1	1	0	RFSP (FA 10095/11)
1	1	1	Reserved

2.3.9 Busy Conditions

A busy condition will not normally exist for the peripheral device interface since the message flow control is performed by the protocol. When the peripheral device has received a complete message,

as denoted by the ETX character, it sends a series of response characters back to the BC. The BC will not send another message to the peripheral device until it receives the final X-ON (11 hex) response character, or a time-out occurs.

2.3.10 Retransmission Conditions

The only time a message is retransmitted is when it has been received by the peripheral device with a parity error.

Messages transmitted over the asynchronous peripheral interface are checked for parity by the receiving end on a character by character basis. Characters received by the peripheral device with a parity error will be printed or displayed by the peripheral device (RFSP or CRT) as a special parity error symbol. The peripheral device response sequence will include a NAK (15 hex) instead of an ACK (06 hex).

When the BC detects the NAK response from the peripheral device, it will attempt to determine the cause of the problem by requesting the peripheral device status byte. If the problem was due to a parity error, it will retransmit the complete original message to the peripheral device. If the peripheral device still does not respond correctly, the BC will discard the original message which will cause the control unit (PCU or RCU) to time-out and reroute if appropriate.

If the NAK response was due to anything other than a parity error, such as an offline, out of paper or fault condition, the message will be discarded and not resent, again causing a control unit time-out.

After discarding the message, the BC will continue to periodically request the status byte from the peripheral device in an attempt to reestablish communication.

2.3.11 Interface Time-Out Conditions

If the peripheral device fails to issue its response within the maximum time-out periods described in paragraph 2.3.7, the BC will time-out and discard the message. This will cause the control unit (PCU or RCU) to reroute the message if appropriate.

2.3.12 Error Conditions

Several error conditions can occur on the peripheral device interface; the following table lists the errors as well as the corrective action to be taken by the BC:

Error Condition	Corrective Action taken by BC
Device not present, or not responding to messages	BC updates internal status byte to indicate the device is not present
Parity error received:	
RANK input	Character changed to special parity error symbol
Response sequence	BC ignores the response, no Text Acknowledge issued
NAK response returned:	BC will request peripheral status byte
Parity error	BC will retransmit the message one time, then abort [Note 1]
Offline	BC will abort the message [Note 2]
Out of paper	BC will abort the message [Note 2]
Device fault	BC will abort the message [Note 2]

Error Condition	Corrective Action taken by BC
Invalid response returned	BC will abort the message [Note 2]
Response time-out occurred	BC will abort the message [Note 2]

NOTES

1. If the peripheral device responds correctly to the retransmitted message, no error condition exists. If the retransmission is not successful, see note 2.

2. The BC will update its internal status byte to indicate that the peripheral device is not available and relay this information to the control unit via the LAN.

2.3.13 Resetting the Peripheral Device Interface

The BC issues a Request Peripheral Status message (see paragraph 6.1.1.3) to the peripheral device approximately every five seconds, whether or not there is any other message activity. This way, the BC is constantly aware of the status of the peripheral device and knows within a short period of time if it has been disconnected or has failed.

If a peripheral device failure or disconnect is detected, the BC updates an internal status byte and informs the control unit (PCU or RCU). The control unit will mark the peripheral device as down and will not send messages to it until a time when the BC is able to reestablish communication with the peripheral device.

The BC continually requests the peripheral status byte on a periodic basis, irregardless of whether the peripheral device is present or what its internal operating state may be.

The BC can reestablish the interface in one of two ways:

1. Peripheral Device Reconnected — Upon power up, following successful completion of its internal diagnostics, the peripheral device sends a non-solicited X-ON to the BC. The BC in turn executes a startup sequence as defined in section 3.0.

2. Error Condition Corrected — When the error has been corrected, or no longer exists, such as an out of paper or offline condition being cleared, the peripheral device will return a clean status byte when requested by the BC. The BC will update its internal status byte and inform the control unit that the peripheral device is again available to accept messages.

3.0 STARTUP, STARTOVER OPERATION

3.1 GPO INTERFACE

The GPO startup and startover operations are implemented through the use of the GPO setup and operational control commands.

3.1.1 GPO System Startup

The GPO system startup procedure consists of the issuance of initilization commands to the GPO hardware and the initialization of the variables used by the GPO firmware.

3.1.2 GPO Startovers

The GPO startover procedures are invoked when any of the following conditions exist:

a. GPO abort condition

b. Parity error received by control unit

c. Overrun condition detected by control unit

d. Checksum mismatch between primary and secondary control unit

e. Message received with incorrect format

3.1.3 GPO Error Recovery

Whenever an error condition exists on the GPO interface, the control unit will raise the appropriate device status line, depending upon the type of error, to inform the NAS computer Host. The control unit will discard any partial message it may have received prior to receiving the error condition, perform a hardware diagnostic loop-back test on the GPO interface logic, and wait for the Host to resend the message. If the diagnostic test reveals a failure, or if the same error occurs in two successive transmissions of the same message, the system error handler will be notified, and an error message will be sent to the front panel of the control unit and to the NAS computer Host via the GPI interface.

A failed GPO circuit in the primary control unit will not cause a control unit switch to occur. Likewise, if the source of the failure cannot be located, it is the responsibility of the NAS computer Host to switch to the backup control unit if it is deemed necessary.

3.2 GPI INTERFACE

The GPI startup and startover operations are implemented through the use of the GPI setup and operational control commands.

3.2.1 GPI System Startup

The GPI system startup procedure consists of the issuance of initialization commands to the GPI hardware and the initialization of the variables used by the GPI firmware.

3.2.2 GPI Startovers

The GPI startover procedure consists of testing DCL1 and waiting until it is active. Following the detection of an active DCL1, the first character of the next message is sent to the NAS computer Host.

3.2.3 GPI Error Recovery

Whenever a parity error is detected by the Host, it will activate DCL3 at the end of the message to request a retransmission from FDIO. Upon detecting this condition, the control unit will perform a diagnostic self-test on the GPI interface logic and resend the message to the Host. If the diagnostic test reveals a failure, or if the parity error occurs in two successive transmissions of the same message, the system error handler will be notified, and an error message will be sent to the front panel of the control unit. It will be the responsibility of the Host to switch to the backup control unit if parity errors on the GPI interface continue. This can be accomplished by sending an Invoke Secondary message (see paragraph 5.1.4) or raising DCL1, DCL3, and DCL4 which will result in a forced switch.

3.3 PERIPHERAL DEVICE INTERFACE

The peripheral devices are initialized for proper FDIO operation by the control unit (PCU or RCU) by sending appropriate initialization messages. Startover and error recovery procedures are performed in the same manner.

3.3.1 Peripheral Device Interface Startup

For the peripheral device interface to be operational, three initialization operations must occur:

1. BC hardware/channel initialization
2. Peripheral device power up initialization
3. Peripheral device set up

3.3.1.1 BC Hardware/Channel Initialization. The BC initializes the peripheral device interface by performing the setup operations on the asynchronous communications controller and the baud rate generator as described in paragraph 2.3.3.

3.3.1.2 Peripheral Device Power Up Initialization. When the peripheral device is powered up, it performs an internal self test and initialization process. If there are no abnormalities, it issues an X-ON to the BC to indicate it is ready for FDIO operation.

3.3.1.3 Peripheral Device Setup. Following power up, the peripheral devices must be setup for proper operation with FDIO. Depending on the specific peripheral device, different setup messages are sent by the control unit. A complete description of the setup messages can be found in section 6.0.

3.3.1.3.1 RFSP 1 1/3 Inch Strip. Enroute RFSPs attached to PCUs and RFSPs used in the oceanic confiuration are initialized by sending down the setup message which performs the following operations:

a. Set up the forms length for 1 1/3-inches

b. Set the tab stops at 11, 17, 38, 44, 64, and 70 [note]

NOTE

The tab stops represent the position prior to where the printer actually prints. A tab stop at position 11 means that a printable character following the tab will actually print in position 12.

3.3.1.3.2 RFSP 1 Inch Strip Remote RFSPs attached to domestic RCUs are initialized by sending down the setup message which performs the following operations:

a. Set up the forms length for 1-inch

b. Set the tab stops at 14, 21, 31, 61, 65, and 70 [note 1,2]

c. Set the tab stops at 9, 14, 21, 31, 40, 57, and 70 [note 1,3]

NOTES

1. The tab stops represent the position prior to where the printer actually prints. A tab stop at position 14 means that a printable character following the tab will actually print in position 15.

2. These tab settings will be sent to the printer if full strips are requested through RECN on the front panel of the control unit.

3. These tab settings will be sent to the printer if half strips are requested through RECN on the front panel of the control unit.

3.3.1.3.3 CRT. CRTs attached to RCUs are initialized by sending down the following sequences of messages:

a. **CLEAR_CRT** — This message clears the CRT screen.

b. **ERASE_LINE_25** — This message clears the 25th line on the CRT (the bottom line).

c. **CRT_DIVIDER** — This message puts the divider lines on the CRT screen to separate the display areas.

d. **SCROLL_AREA** — This message sets up lines 1-15 on the CRT to scroll (domestic configuration only).

e. Set tab stops at 15, 24, 36, 67, 73 and 79 [note] (domestic configuration only).

f. Set tab stops at 12, 18, 34, 41, 72 and 79 (oceanic configuration only).

NOTE

The tab stops represent the position prior to where the character is displayed. A tab stop at position 14 means that a displayable character following the tab will actually print in position 15.

Figure 3-1 shows the layout of the CRT display following initialization in the domestic configuration and figure 3-1A shows the layout in the oceanic configuration.

3.3.1.3.4 RANK. There are no setup sequences for a RANK.

3.3.1.3.5 Maintenance Channel. The maintenance channel is initialized by sending down the message **MAINT_SETUP** which enables the RFSP front panel configuration mode setup.

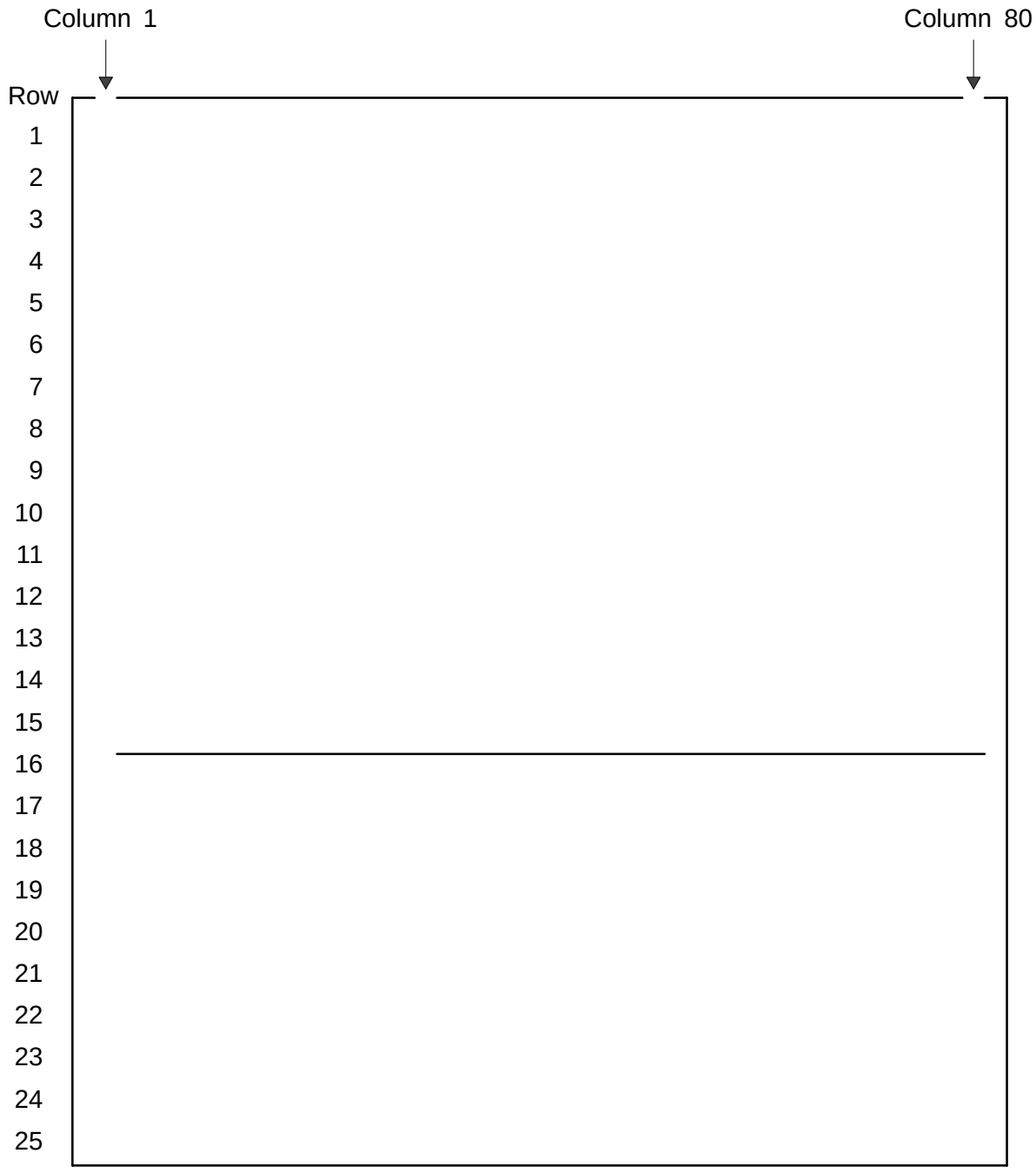


FIGURE 3-1. STANDARD INITIALIZED CRT DISPLAY

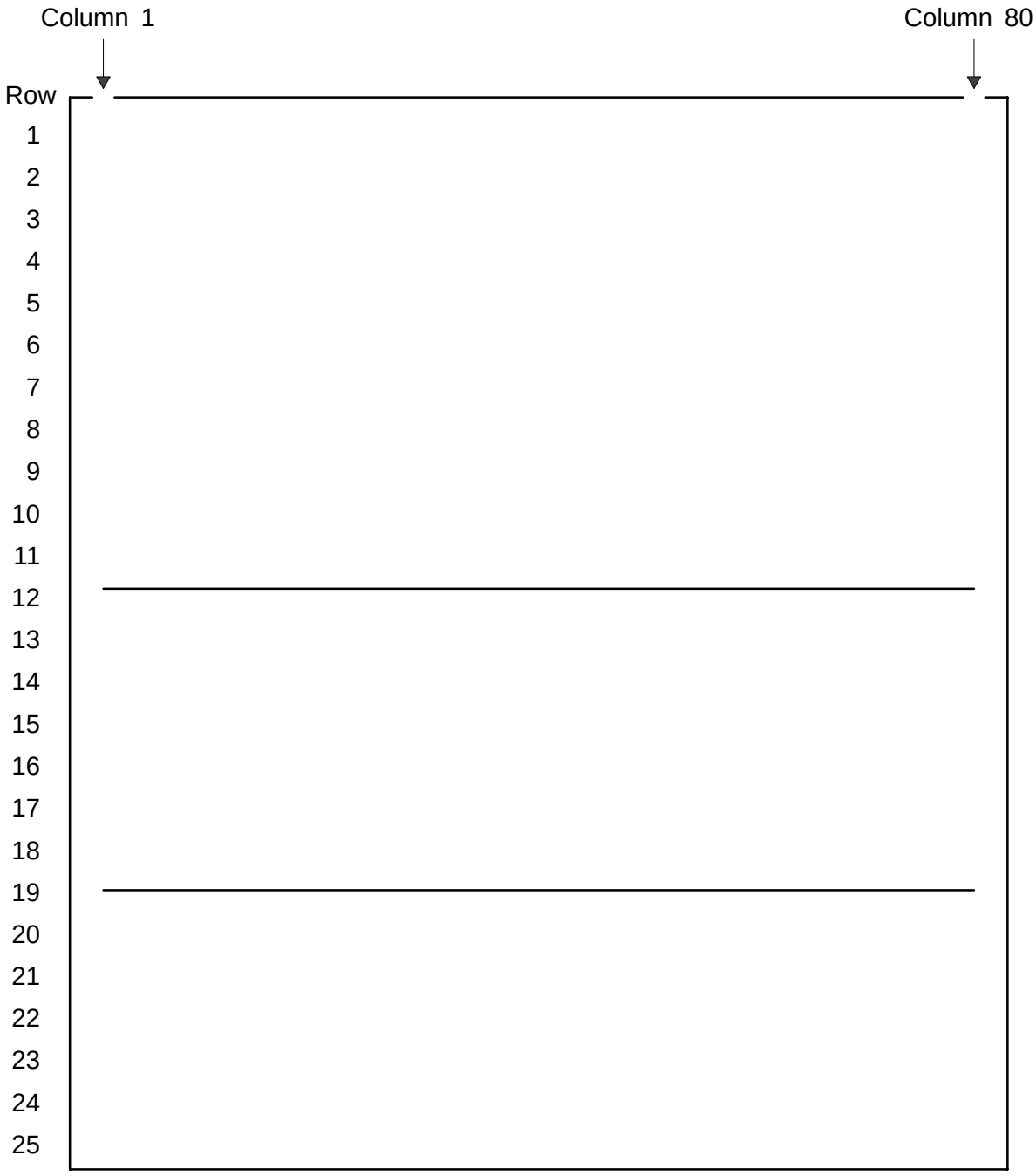


FIGURE 3-1A. OCEANIC INITIALIZED CRT DISPLAY

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3.3.2 Peripheral Error Recovery

Errors on the peripheral device interface can be associated with either transmitted messages and their response or non-solicited input messages.

3.3.2.1 Transmitted Messages. If an error occurs during the transmission of a message to a peripheral device, or the associated response sequence, one of the following error recovery operations will be performed:

a. Message Retransmission — If the error was due to a received parity error by the peripheral device, the message will be retransmitted (see paragraph 2.3.10).

b. Peripheral Reinitialization — If the error cannot be corrected by retransmission (i.e., device offline, a device check or an invalid response sequence), the BC will discard the message and inform the control unit that the peripheral device is not available. This will cause the control unit to time-out and, if appropriate, reroute the message.

The BC will periodically attempt to reestablish communication with the peripheral device, and when successful will force the control unit to reissue the peripheral device setup sequence (see paragraph 3.3.1.3).

3.3.2.2 Input Messages. If a parity error occurs on a non-solicited input message, one of the following error recovery operations will be performed:

a. RANK Input — If a parity error occurred on a RANK input character, the character will be changed to the special RANK parity symbol as described in appendix B.1.2.1.

b. Peripheral Reinitialization — If a parity error occurred on a non-RANK Input (such as a response character), that peripheral device will be classified as down by the BC and the control unit. When the BC is able to reestablish communication, it will cause the control unit to reissue the setup sequence to the peripheral device (see paragraph 3.3.1.3).

4.0 FDIO MESSAGE DESCRIPTIONS

This section defines the messages and addressing techniques that will be used for communication between the Host system and the FDIO system.

4.1 FDIO MESSAGE FORMATS

FDIO messages will be received in Extended Binary-Coded Decimal Information Code (EBCDIC) from the Host, over the GPO interface, converted to an internal format for routing and reformatted into ADCCP frames for transmission to the BCs and peripheral devices. FDIO messages received from peripheral devices will be formatted into ADCCP frames by the BC for transmission to the CCU (via an RCU) or PCU and converted to EBCDIC (where necessary) for transmission to the Host over the GPI interface. The information will be contained in one of the following three types of messages:

1. IBM messages (Host ↔ CCU and PCU)

2. Internal FDIO messages

3. ADCCP messages

FDIO messages will consist of several fields, each containing message address, type, and textual information.

4.1.1 IBM Messages

FDIO has been designed to operate with several application programs running on the Host computer system:

NAS — National Airspace System Program
SCOPE — System Checkout of Peripheral Equipment Program
T&M — Test and Maintenance

A common trait of these application programs is that they all use the GPI and GPO interfaces between the PAMRI adapters and the FDIO control units for message communication. Since the FDIO firmware processes these messages in a generic fashion, they are referred to within this document as IBM messages, as opposed to NAS messages, SCOPE messages, or T&M messages.

There are two formats for IBM messages which are embedded in a 6-field message block as illustrated in figure 4-1.

1. IBM Output Messages — Those messages received from the Host via the GPO interface.

2. IBM Input Messages — Those messages sent to the Host via the GPI interface.

IBM Output Messages

FIELD	1	2	3				4	5		6	
			← Destination Address →					← Text →			
	Prior	Space	FDIO Addr 1	FDIO Addr 2	Bkup 1	Bkup 2	CR/LF	STX	Type	Text	ETX
	(2)	(1)*	(1)	(1)	(1)	(1)	(2)	(1)	(1)	Note	(1)

IBM Input Messages

FIELD		3				4	5		6	
		← Originator Address →					← Text →			
	FDIO Addr 1	FDIO Addr 2	Bkup 1	Bkup 2	CR/LF	STX	Type	Text	ETX	
	(1)*	(1)	(1)	(1)	(2)	(1)	(1)	Note	(1)	

*Numbers in parentheses indicate how many 8-bit characters are contained within the field.

NOTE

The maximum number of characters in the text field is 1,700 and ends with an ETX character (03 hex).

FIGURE 4-1. IBM MESSAGE FORMAT

4.1.1.1 Peripheral Device Addressing. The peripheral device address will be defined as a local address within each control unit (CCU, PCU, and RCU) and will uniquely specify a peripheral device that is attached to a BC on the LAN. The device address will be the same address as the BC (hardware selected via S2, the 7-position rocker-switch on the BC).

The Host will address and communicate with peripheral devices by placing the device number listed below into the Addr 1, Addr 2, Bkup 1, and Bkup 2 fields of the message as defined in the following paragraphs:

Device No.	[Hex]	Device Description
1 - 10	[1 - 0A]	RFSP at RCU
11 - 15	[0B - 0F]	CRT at RCU
16 - 20	[10 - 14]	RANK at RCU
21	[15]	Maintenance Channel at RCU
1 - 28	[1 - 1C]	RFSP at PCU or Modem at CCU
29	[1D]	Maintenance Channel at PCU

These address assignments dictate that only RFSPs be connected as physical devices 1-10 on the LAN, CRTs will be devices 11-15, and RANKs will be devices 16-20. There can be gaps in the address definitions, such as having only RFSPs 1, 2, and 8, or CRTs 11, 14, and 15.

4.1.1.2 FDIO Addr 1 and 2. In order to specify a complete address within the FDIO system, it is necessary to specify multiple address parameters. The address parameters determine which control unit will receive (or has originated) the message. FDIO Addr 1 consists of one character and specifies (in binary) the primary FDIO address such as the CCU or PCU itself, or one of the devices [i.e., modem or RFSP] on the CCU or PCU LAN. FDIO Addr 2 also consists of one character and specifies (in binary) the secondary FDIO address (i.e., the RCU itself or one of the peripheral devices on the RCU LAN).

The two address fields are defined as follows:

Addr 1	[Hex]	Primary FDIO Address
0	[0]	Message to (CCU or PCU)
1 - 28	[1 - 1C]	Message to RCU (if directed to CCU)
1 - 29	[1 - 1D]	Message to peripheral device (if directed to PCU)
30 - 255	[1E - FF]	Invalid address

Addr 2	[Hex]	Secondary FDIO Address
0	[- 0]	Message to RCU
1 - 21	[1 - 15]	Message to peripheral device (at RCU)
22 - 255	[16 - FF]	Invalid Address

The two address fields provide the following decoded address information:

Addr 1	Addr 2	Communication Is With:		
0	X	Host	↔ CCU, PCU	(base)
1 - 28	0	Host	↔ RCU	(base)
1 - 29	X	Host	↔ PCU	(device)
1 - 28	1 - 21	Host	↔ RCU	(device)

4.1.1.3 Bkup 1 and 2. Bkup 1 and 2 each consist of one character, and contain different information depending on the specific type of message being sent (see paragraph 4.1.1.6 and section 5.0 for information pertaining to the message type). The following applies:

a. Text Message (output) — Bkup 1 and 2 each will contain the address (in binary) of a device that will be used for message rerouting. If the primary output device is unable to print the message, it will be rerouted to the primary backup device as specified by bkup 1. If that device is also unable to print the message, and the control unit is a PCU, the message will be rerouted to the secondary backup device as specified by bkup 2 (there is only one backup device in an RCU). If the message cannot be printed, it will be returned to the Host as a Text Acknowledge with Error message.

b. Text Message [Accept, Reject, or Error] (output) — When an Accept, Reject, or Error message is sent to the RCU in response to an input message from a RANK, bkup 2 will specify the

address of the RANK (16-20) on which the message was entered. This will enable RCU firmware to determine to which echo device (CRT or RFSP) the message should be sent.

c. Text Acknowledge (input) — When a Text Acknowledge message is returned to the Host, the bkup 1 will indicate which peripheral device actually printed (displayed) the text message. If the bkup 1 is zero, the message will have been printed by the primary output device as specified by fields addr 1 and 2, without any rerouting having occurred.

4.1.1.4 Priority Field. The priority field will consist of two EBCDIC characters and will not be used by the FDIO system.

4.1.1.5 Space. This field will contain an EBCDIC space character (40 hex) and will not be used by the FDIO system.

4.1.1.6 CR/LF. This field contains an EBCDIC carriage return and line feed pair (15, 25 hex).

4.1.1.7 STX. This field contains an EBCDIC STX character (02 hex).

4.1.1.8 Type. In addition to new addressing techniques, there is a requirement for messages other than flight data messages to be sent to the CCU, PCU, and RCU. The message type consists of one binary character and specifies the message type. See section 5.0 for a description of the message types.

4.1.1.9 Text Field. The text field contains the IBM text message in EBCDIC to be printed.

4.1.1.10 ETX. All messages received from the Host contain an EBCDIC ETX character (03 hex) as the last character.

4.1.2 Internal FDIO Message Format

This section defines the messages and addressing techniques that will be used for communication between FDIO firmware tasks. Although this section is beyond the scope of this document, it is included to provide additional information that should assist in understanding the basic I/O operation of the FDIO system.

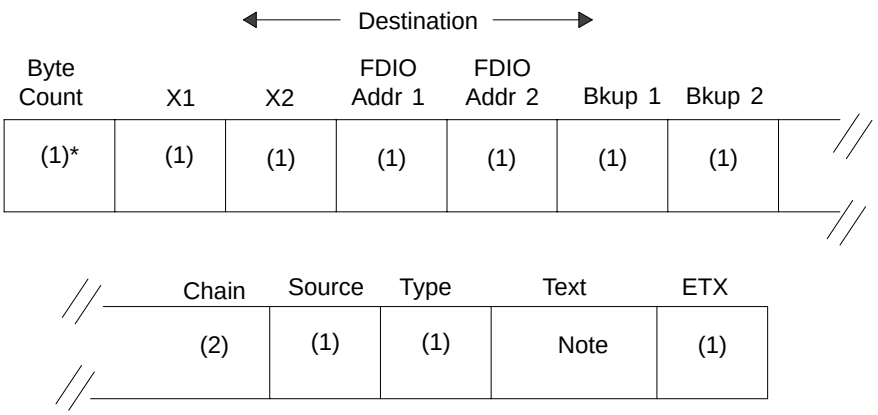
There are two basic types of internal messages, depending on the general direction in which they are traveling:

1. Outward Message — This message is characterized by a general flow from the Host towards the RCU or PCU peripheral devices. An example of an outward message is a Text message initiated by the Host and sent to an RCU peripheral device. The format for this type of message is shown in figure 4-2.

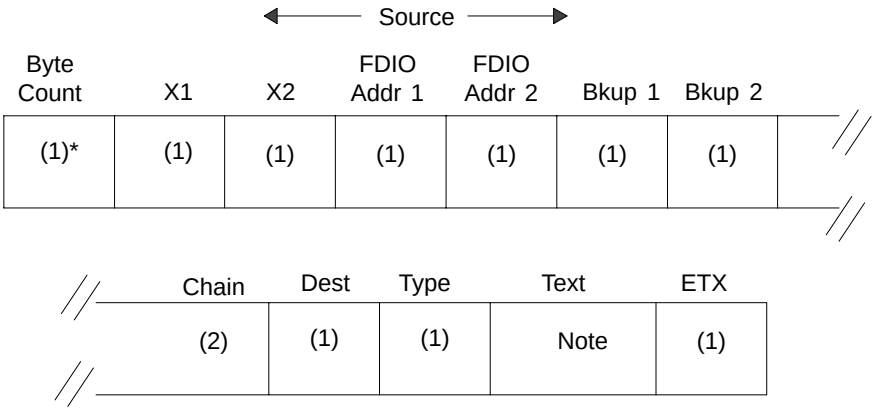
2. Inward Message — This message is characterized by a general flow from the RCU peripheral device towards the Host. An example of an inward message is a RANK input message initiated at the RCU and sent to the Host. The format for this type of message is shown in figure 4-2.

4.1.2.1 Byte Count. This field contains a 1-byte binary byte count that will be calculated when the message is received at a control unit. The byte count indicates the length of the message contained within the current memory block in bytes, beginning with the X1 field through the final byte of the text field. This count is used by the transmission algorithms when determining the number of bytes to be transmitted.

Outward Message Format



Inward Message Format



*Numbers in parentheses indicate how many 8-bit characters are contained within the field.

NOTE

The maximum number of characters in the text field is 117. Up to 1,700 text characters are available for the entire message by chaining several blocks together.

FIGURE 4-2. INTERNAL MESSAGE FORMAT

4.1.2.2 X1 Field. This field consists of one byte and will be added by the ADCCP transmission routines as the single octet ADCCP address byte.

4.1.2.3 X2 Field. This field consists of one byte, corresponding to the ADCCP control byte. The ADCCP transmission routines will add send and receive variables to this byte.

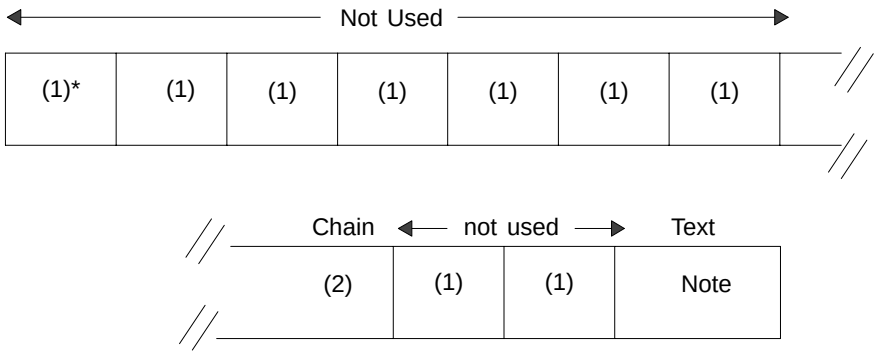
4.1.2.4 FDIO Addr 1 and 2. Refer to paragraph 4.1.1.2 for a description of these.

4.1.2.5 Bkup 1 and 2. Refer to paragraph 4.1.1.3 for a description of these.

4.1.2.6 Chain. This field is used when the entire FDIO message cannot fit into a single 128-byte memory block (primary message block). This field consists of a 16-bit (2 bytes) offset pointer to another 128-byte block (secondary message block) containing an additional portion of the message. The secondary message block contains up to 117 bytes of text characters plus eleven (11) bytes of overhead (see figure 4-3). Of the eleven bytes of overhead, only the chain bytes are defined, allowing several secondary message blocks to be chained together sequentially from a primary message block. In this manner, long multi-block messages can be maintained within the control unit.

Long messages are only blocked while they exist within the control unit. When the messages are transmitted over the LAN, the primary message block, together with the text portions of any secondary message blocks are transmitted as a single contiguous message. For simplicity, the chain bytes continue to occupy space in the transmitted message (see figure 4-3).

A control unit, upon receiving a long ADCCP message will partition it into blocks and redefine the unused chain bytes based upon its own current memory utilization.



*Numbers in parentheses indicate how many 8-bit characters are contained within the field.

NOTE

The maximum number of characters within the text field of a single block is 117.

FIGURE 4-3. SECONDARY MESSAGE BLOCK FORMAT

4.1.2.7 Source or Destination. This field consists of one byte and indicates the source of an outward message or the destination of an inward message. Setting the upper bit to 8 will indicate that a checksum is present in the message. This field is defined as follows:

Content	Source/Dest
0	NAS Computer
1	CCU/PCU Diagnostic Task
2	RCU Diagnostic Task
3	Reserved
4	RCU Message Entry (non-response)
5	Non-response (Note)
6	Reserved
7	Reserved

NOTE

A non-response message sent to a peripheral device will not result in a Text Acknowledge message. Examples would be the Text message that displays the words **MESSAGE PENDING** on a CRT, or the echo of a RANK character on an RFSP or CRT.

4.1.2.8 Type. Refer to section 5.0 for a description of message types.

4.1.2.9 Text. Some messages contain a text field containing information coded in American Standard Code for Information Interchange (ASCII).

4.1.2.10 ETX. All internal messages contain an ETX (03 hex) as the last character of the message.

4.1.3 ADCCP Messages

This section outlines those ADCCP messages (frames) that will be used for communication within FDIO. Although this section is beyond the scope of this document, it is included to provide additional information that should assist in understanding the basic I/O operation of the FDIO system.

The ADCCP protocol will be used on the following communication interfaces:

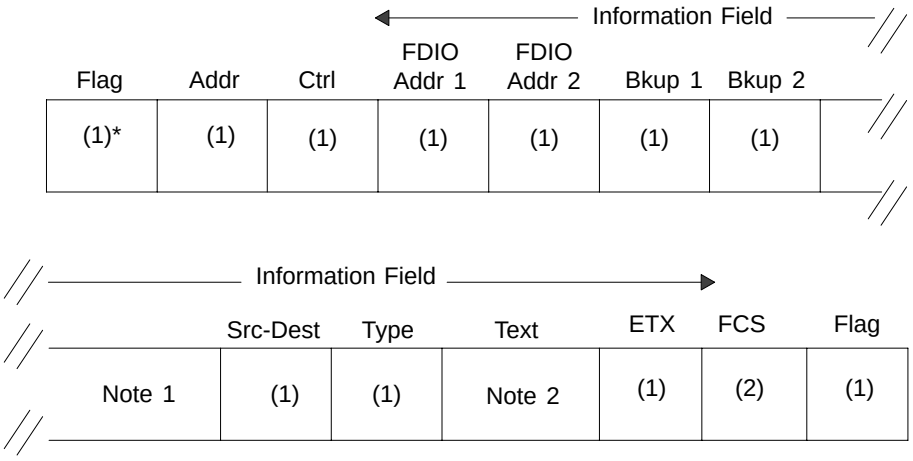
CCU, PCU, RCU ↔ BC (via LAN)

BC ↔ RCU (via modem)

The messages transmitted using the ADCCP protocol use a variation of the internal message format; the byte count field will not be transmitted (it will be recalculated when the message is received at the destination) and the FDIO address, backup, chain, source or destination, type, text, and ETX fields will be contained within the ADCCP text field. The format for ADCCP messages (frames) is illustrated in figure 4-4.

4.1.3.1 Flag. The first and last bytes of the ADCCP frame are flag sequences consisting of the following binary bit pattern: **01111110**.

4.1.3.2 Addr. This field consists of one byte and will contain the single octet ADCCP address byte. This field indicates to which BC (and peripheral device) the message will be sent.



*Numbers in parentheses indicate how many 8-bit characters are contained within the field.

NOTES

1. Two chain bytes used in the internal message format are unused by the ADCCP frame and contain zeroes.

2. The maximum number of text characters in the text field is 1,700.

FIGURE 4-4. ADCCP MESSAGE FORMAT

4.1.3.3 Ctrl. This field will consist of one byte and will contain the ADCCP control byte. The ADCCP transmission routines will add send and receive sequence numbers to this byte.

4.1.3.4 Information Field. This field contains the following fields of the internal message format:

a. FDIO addr fields 1 and 2

b. FDIO bkup fields 1 and 2

c. chain field

d. source or destination field

e. message type field

f. FDIO text field

g. ETX character

4.1.3.5 FCS. The FCS occupies the two bytes just prior to the closing flag and is used for error detection purposes. The contents of the address, control, and information fields are included in the calculation of the FCS sequence.

4.2 COMPARISON OF MESSAGES

This section compares the three message formats and describes what changes are required for conversions.

4.2.1 Formats

Formats of outward and inward messages are shown in figures 4-5 and 4-6 respectively.

4.2.2 Conversion Requirements

FDIO firmware will perform the steps necessary to convert the messages between the three formats.

4.2.2.1 Host Format to Internal Format. A message received from the Host must be modified before it can be used in the FDIO system. The following fields must be converted:

a. The priority and space fields are not used by FDIO. The three bytes occupied by these two fields will become the byte count, X1 and X2 fields. The byte count field will be determined by the FDIO receiving firmware when the IBM message is received, and the X1 and X2 fields will be set to zero (to be used later by the ADCCP protocol firmware).

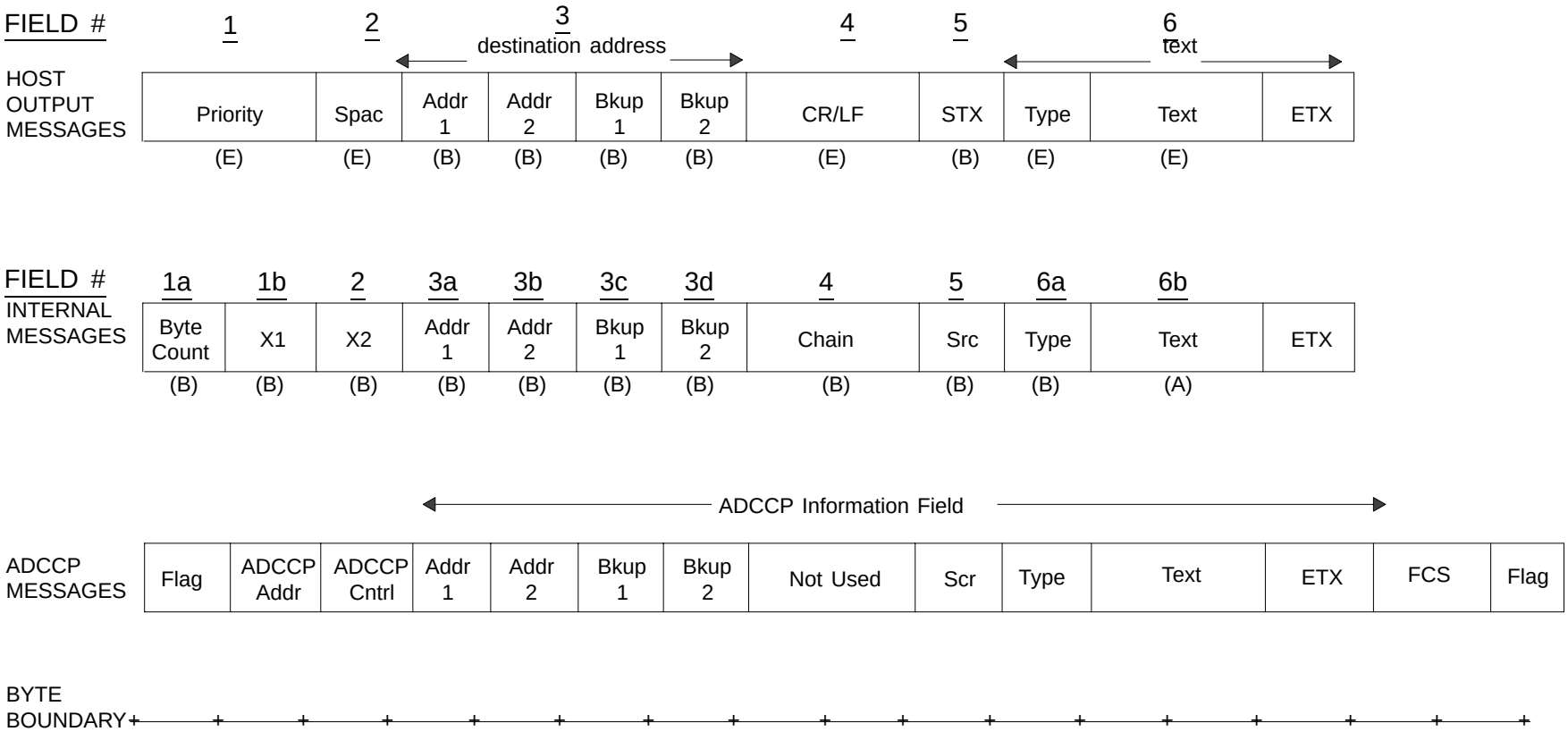
b. The CR/LF field must be changed into the chain field. If the message is too long to be contained in one block of memory, this field will contain the pointer to another memory block where the remainder of the message will be located. If the message fits in the single block, this field will be set to zero.

c. The STX field is not used by FDIO, and will become the source or destination field. The source or destination field is an 8-bit field.

d. The EBCDIC text field will be converted to ASCII.

e. Eight nulls (0 hex) will be attached to the beginning of the text field to allow room for CRT cursor positioning control characters that may be added at a later time.

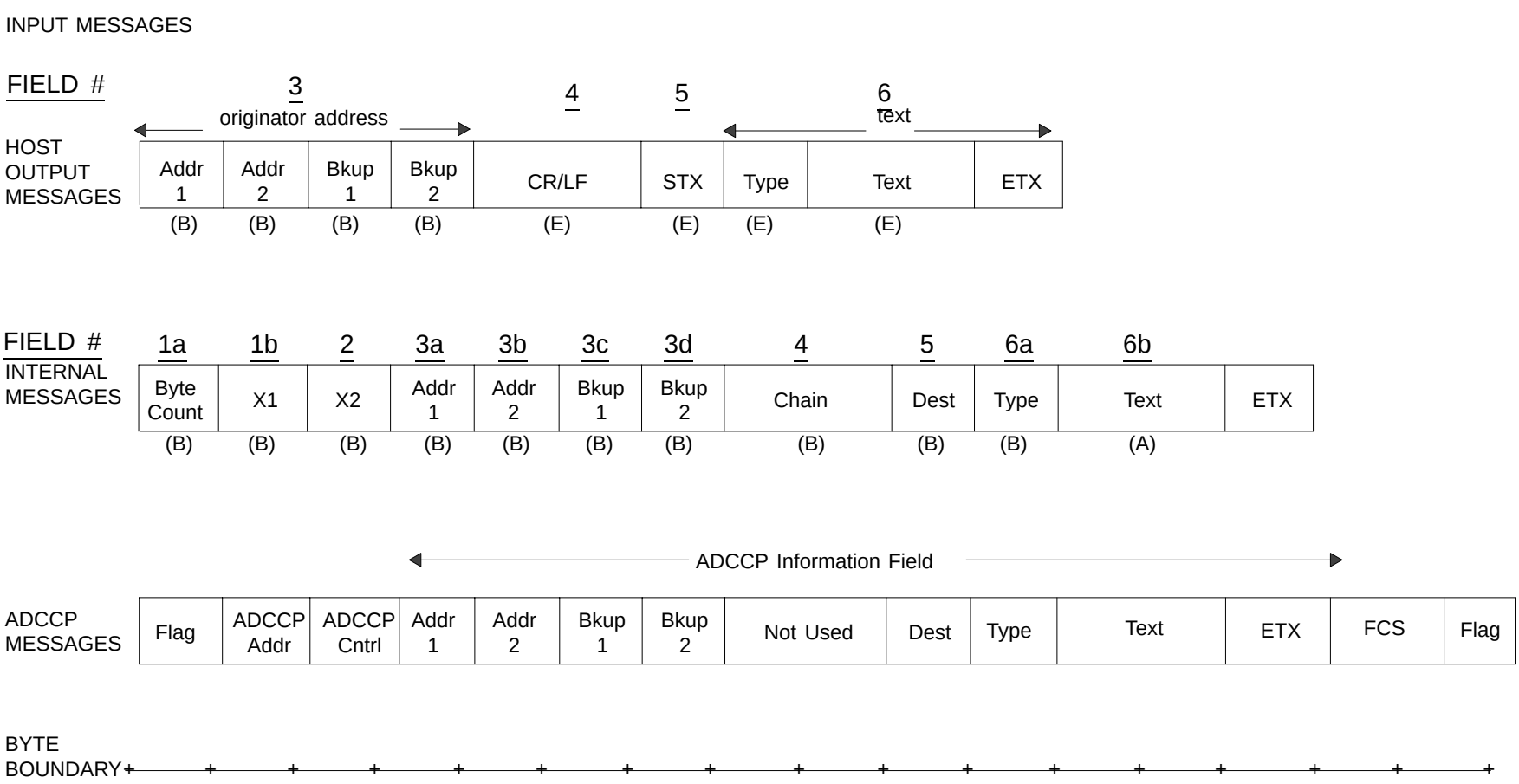
OUTPUT MESSAGES



FIELD CODING

E . . .EBCDIC
A . . .ASCII
B . . .BINARY

FIGURE 4-5. OUTWARD MESSAGE FORMATS



FIELD CODING

E . . .EBCDIC
A . . .ASCII
B . . .BINARY

FIGURE 4-6. INWARD MESSAGE FORMATS

4.2.2.2 Internal Format to Host Format. An internal message must be modified before it can be sent to the Host. The following fields must be converted:

a. Byte count, X1 and X2 are not transmitted to the Host; the first character transmitted to the Host is Addr 1.

b. The chain field must be converted to an EBCDIC CR/LF sequence for transmission to the Host. FDIO firmware will concatenate multiple-block messages and send the entire message to the Host if additional blocks are indicated by this field.

c. The source or destination field must be converted to the EBCDIC STX character.

d. Any ASCII text information in the text field must be converted to EBCDIC.

4.2.2.3 Internal Format and ADCCP. The internal format is directly compatible with the ADCCP format with the exception that the byte count field will not be transmitted. The X1 field will become the ADCCP address field and will contain the address of the BC on the LAN. The X2 field will become the ADCCP control field and will contain the ADCCP control byte. All the remaining fields are considered part of the ADCCP text field [all internal messages are transmitted as ADCCP Information (I) frames].

5.0 MESSAGE TRANSFERS OVER GPI AND GPO INTERFACES

Control and information messages are transmitted between the Host and the CCU or the Host and the PCU via the GPI and GPO interface channels. Messages consist of several fields, with each field containing specific control or text information.

5.1 OUTPUT MESSAGES FROM HOST

The Host sends information and control messages to CCUs, PCUs, and RCUs (via CCUs) over the GPO interface. The type field within the IBM message format specifies the type of output message being sent.

The following IBM output message types are defined:

Generic Message Type	Message Description
0X	Text
1X	Disable Front Panel
2X	Enable Front Panel
3X	Invoke Secondary
4X	Query Primary
6X	Poll FDIO
7X	SCOPE
8X	Utility Messages

5.1.1 Text

Text messages result in the transfer of flight data messages between the Host and the FDIO system. Text messages consist of flight strip data from the Host and are directed to an RFSP or CRT. The address bytes must specify a valid peripheral device. All flight strip messages will be acknowledged by FDIO. The least significant digit of the message type determines the type of flight strip data as follows:

Message Type	Contents of Text	
00	FDIO text message	[Note 1]
01	Weather message	[Note 1]
02	General information message	[Note 1]
04	Accept response to RANK input	
05	Reject response to RANK input	
06	Error response to RANK input	
08	Update pending message (oceanic configuration only)	

Generic Message Type: 0X
Response from FDIO: Text Acknowledge message

Message Formats:

	Addr 1	Addr 2	Bkup 1	Bkup 2		Type	Text	ETX
[PCU]	1 - 28	0	1 - 28	1 - 28		OX	text	03
[RCU]	1 - 28	1 - 10	1 -10	Note 2		OX	text	03

NOTES

1. A text message can not be addressed to a CRT in the domestic configuration. The message must have a printer address in the header. A text message that is sent to the control unit with an invalid address will return a NAK to the system.

2. Because the RCU will only support one level of rerouting, the Bkup 2 field does not contain peripheral backup information. This field contains **0** unless the message is one of the three RANK response messages (Type = 04,05,06). For a RANK response message, the Bkup 2 field will contain the address of the RANK at which the message was input. The RANK address is used to determine which output device will receive the RANK response message.

5.1.2 Disable Front Panel

This command causes the front panel to ignore local operator-initiated attempts to communicate with the system. The front panel will continue to display messages; however, the keypad input is locked out.

Generic Message Type: 1X
Response from FDIO: Front Panel Status message

Message Formats:

	Addr 1	Addr 2	Bkup 1	Bkup 2		Type	ETX
[CCU/ PCU]	0	X	0	0		10	03
[RCU]	1 - 28	0	0	0		10	03

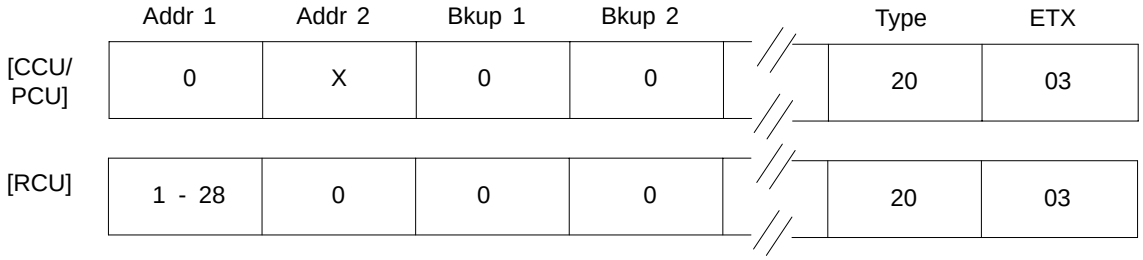
5.1.3 Enable Front Panel

This command causes the front panel to respond to operator-initiated attempts to communicate with the system. The front panel will display messages, and the keypad will be enabled.

Response from FDIO: Front Panel Status

Generic Message Type: 2X
Response from FDIO: Front Panel Status message

Message Formats:

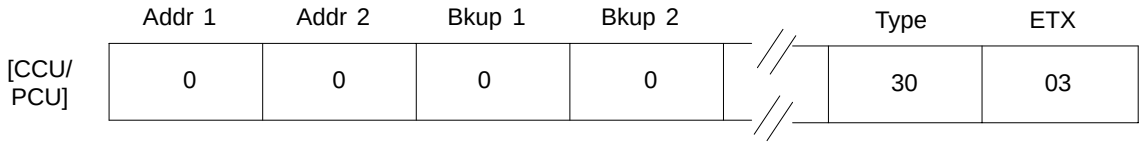


5.1.4 Invoke Secondary

This command, when directed to the CCU or the PCU, causes a control unit switch (i.e., the operating control unit relinquishes control to the secondary control unit).

Generic Message Type: 3X
Response from FDIO: Configuration Status message

Message Format:

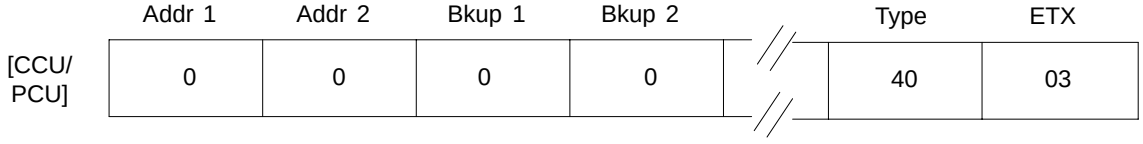


5.1.5 Query Primary

This command causes the CCU or the PCU to send the control unit status to the NAS computer Host.

Generic Message Type: 4X
Response from FDIO: Configuration Status message

Message Format:

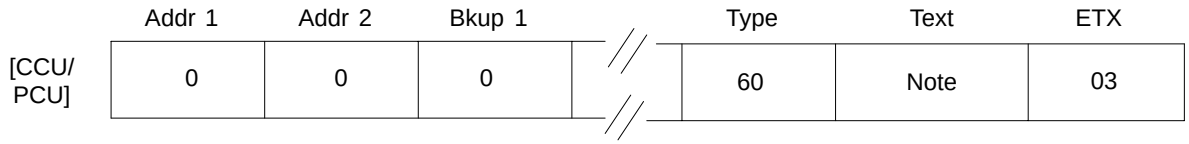


5.1.6 Poll FDIO

This command can be directed to a CCU or a PCU to verify the GPI/GPO interfaces. When polled, the control unit will respond with a Poll Acknowledge.

Generic Message Type: 6X
Response from FDIO: Poll Acknowledge message

Message Format:



NOTE

The type 6X message may include an optional Text field which will be returned as part of the Poll Acknowledge message (see paragraph 5.2.6).

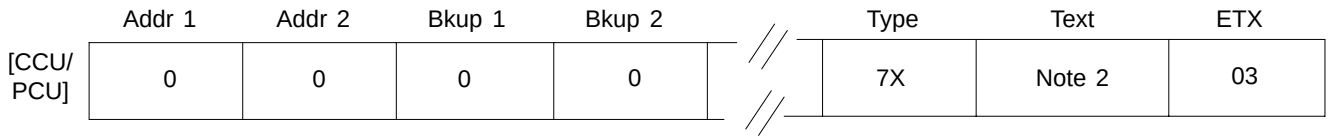
5.1.7 SCOPE

SCOPE messages (commands) are issued to the CCU and PCU for the purpose of testing the GPI and GPO interfaces and the peripheral devices attached to the PCU and RCU. The least significant digit of the message type determines the specific SCOPE command being issued.

Message Type	Description of SCOPE Command
70	Initiate SCOPE mode and begin peripheral and interface testing.
73	Request interim counts.
74	End peripheral and interface testing and return no counts.
77	End peripheral and interface testing, exit SCOPE mode and return counts.
79	SCOPE/System Reset [Note 1].

Generic Message Type: 7X
Response from FDIO: Scope Response message

Message Formats:



NOTES

1. A SCOPE type 79 message causes the control unit to perform a system reset which will delete all messages within the system and initialize the FDIO firmware. No response message will be sent to the Host as a result.

2. Only SCOPE message type 70 will contain information within the text field. All other SCOPE commands will contain no text field.

SCOPE message type 70 contains 32 bytes of coded EBCDIC information within the text field. The definition of the characters is as follows:

byte 0, 29-31 — not used

bytes 1-28 — Each byte position corresponds to an RCU (if the command is sent to a CCU) or an RFSP En Route (E) (if the command is sent to a PCU). An EBCDIC value of **1** enables the particular RCU or RFSP for SCOPE operation, and an EBCDIC value of **0** will disable SCOPE operation.

While in SCOPE mode, all non 7X type commands received from the Host will be echoed back to the NAS computer Host as received.

5.1.8 Utility Messages

Utility messages provide for future expansion by allowing for additional message types. At the time of this writing, only the following utility message has been defined:

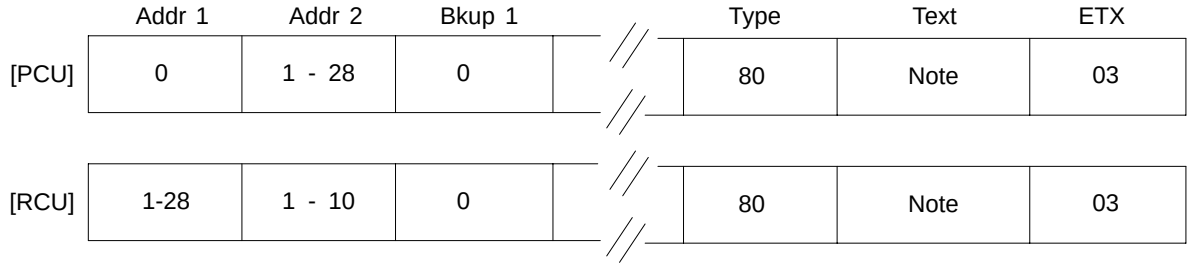
Message Type	Description of SCOPE Command
80	Set RFSP strip eject time-out.

5.1.8.1 RFSP Eject Time-out. This message can be directed to a PCU or an RCU to set the RFSP strip eject time. This time corresponds to the amount of time the RFSP will wait following the printing of a flight strip message before moving the flight strip to a position above the tear bar. The time information is encoded in four EBCDIC characters within the Text field of the message and corresponds to the number of seconds of delay. The maximum time that may be specified is 9,999 seconds (approximately 2.75 hours). If the time parameter is specified as zero (0000), the flight strip eject time-out will be set to infinite and no strip ejecting will be performed.

The time-out parameter is valid for all RFSPs connected to the PCU or RCU. Individual RFSPs at a common control unit will all have identical strip eject time-outs; however, RFSPs at different control units may have different time-outs.

Generic Message Type: 80
Response from FDIO: None

Message Format:



NOTE

The Text field contains four EBCDIC numeric characters representing the flight strip eject time-out from 1 through 9,999 seconds (0 indicates an infinite time-out).

5.1.9 Message Utilization Summary

Table 5-1 illustrates the sequence of all possible output messages.

TABLE 5-1. HOST OUTPUT MESSAGES/RESPONSES

Preceding Input Message from FDIO	Output Message to FDIO	Resulting Input Message from FDIO
—	Text	Text Acknowledge
—	Disable Front Panel	FP Status
—	Enable Front Panel	FP Status
—	Invoke Secondary	Config Status
—	Query Primary	Config Status
—	Poll FDIO	Poll Acknowledge
—	SCOPE	SCOPE Response
—	RFSP Eject Time-out	None

5.2 INPUT MESSAGES TO NAS COMPUTER

IBM input messages are sent over the GPI interface channel to the Host. Input messages allow the Host to receive response and input text messages from the FDIO system.

There are two classes of input messages:

1. Response Message — This class of message is issued by the FDIO system in response to a previously issued IBM message, such as text acknowledge. A response message indicates whether a particular NAS IBM message has been successfully executed.

2. Nonsolicited Input Message — This class of message is issued by the FDIO system when it has new information for the Host. Text and error input messages fall into this category.

The following IBM input message types will be defined:

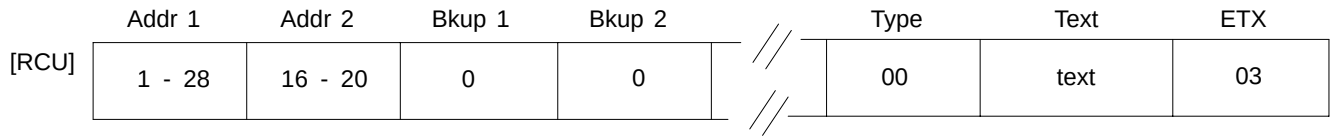
Generic Message Type	Message Description	Class
0X	Text	non-solicited
1X	Text Acknowledge	response
2X	Configuration Status	response
3X	Front Panel Status	response
5X	Errror Status	non-solicited
6X	Poll Acknowledge	response
7X	SCOPE Response	response

5.2.1 Text

A Text message contains textual information that has been entered at a RANK.

Generic Message Type: 0X
Response from IBM: Text (RANK Accept, Reject or Error) message

Message Formats:



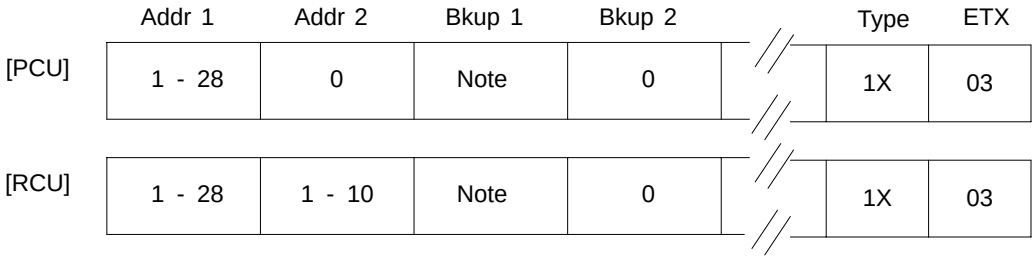
5.2.2 Text Acknowledge

A Text Acknowledge message informs the Host of the result of an IBM initiated output Text message. If the Text message has been processed and successfully printed (displayed) on the intended device or a backup device, a Text Acknowledge message is sent to the Host. Otherwise a Text Acknowledge with Error message is sent.

Message Type	Message Name	Description
10	Text Acknowledge	successfully printed
11	Text Acknowledge with Error	not printed
12	Reserved for internal use	

Generic Message Type: 1X
Response from IBM: None

Message Formats:



NOTE

For a type 10 acknowledge message the Bkup 1 field will contain **0** if the message was printed on the device specified by the Addr 1 and Addr 2 fields. If the message was rerouted, the Bkup 1 field will contain the address of the device that actually printed (displayed) the text message.

5.2.3 Configuration Status

This message is issued in response to invoke secondary backup and query primary commands issued by the Host. The byte immediately following the message type field in the text field indicates which control unit, A or B, is the primary control unit.

Generic Message Type: 2X
Response from IBM: None

Message Formats:

	Addr 1	Addr 2	Bkup 1	Bkup 2	Type	Text	ETX
[CCU/ PCU]	0	0	0	0	20	A/B	03

5.2.4 Front Panel Status

This command is issued in response to an enable or disable front panel command. The byte immediately following the message type field in the text field indicates whether the front panel is presently enabled (E) or disabled (D).

Generic Message Type: 3X
Response from IBM: None

Message Formats:

	Addr 1	Addr 2	Bkup 1	Bkup 2	Type	Text	ETX
[CCU/ PCU]	0	0	0	0	30	E/D	03
[RCU]	1 - 28	0	0	0	30	E/D	03

5.2.5 Error Status

An Error message will be sent to the Host when a control unit detects an error or abnormality within the control unit environment. The text field contains a text string encoded in EBCDIC that will describe the error condition. See appendix C for a complete list of error messages that will be sent to the Host.

Generic Message Type: 5X
Response from IBM: None

Message Formats:

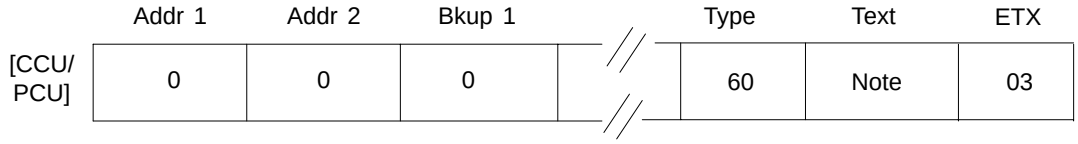
	Addr 1	Addr 2	Bkup 1	Bkup 2	Type	Text	ETX
[CCU/ PCU]	0	0	0	0	50	error text	03
[RCU]	1 - 28	0	0	0	50	error text	03

5.2.6 Poll Acknowledge

This message is sent to the Host by the CCU and PCU in response to a poll command, and indicates that the control unit is present.

Generic Message Type: 6X
Response from IBM: None

Message Formats:



NOTE

If the Poll message (see paragraph 5.1.6) contained text in this optional field, the Poll Acknowledge message will return the same text in this field.

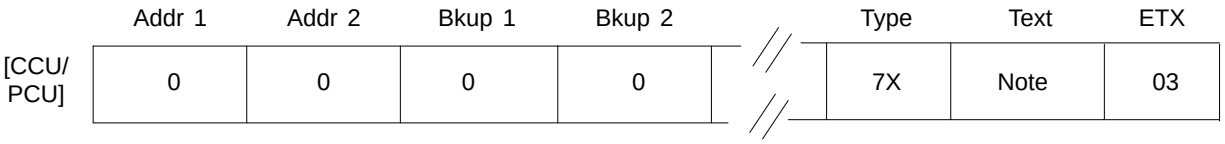
5.2.7 SCOPE Response

The SCOPE response message is sent to the Host in response to a SCOPE command issued by the Host. The SCOPE response will be the same message type as the SCOPE command that is being responded to. The least significant digit of the message type determines the specific SCOPE response being issued.

Message Type	In Response to SCOPE command
70	Initiate SCOPE mode and begin peripheral and interface testing.
73	Request interim counts.
74	End peripheral and interface testing and return no counts.
77	End peripheral and interface testing, exit SCOPE mode and send counts.

Generic Message Type: 7X
Response from IBM: None

Message Formats:



NOTE

Only SCOPE message types 73 and 77 contain information within the text field, all other SCOPE commands will contain no text information.

SCOPE type 73 and 77 messages contain either 224 or 4,480 EBCDIC characters depending on whether the response message originates from a PCU or a CCU. A PCU response includes 28 count

pairs within the text field, one count pair for each of the possible 28 RFSP(E)s. Each count pair consists of two 16-bit counts (four bytes), one representing the number of print attempts to the specific RFSP(E) and the second representing the number of resulting errors. Each four byte count pair is transmitted as eight EBCDIC characters for a total of 224 characters.

A CCU response includes 560 count pairs within the text field, one count pair for each of the possible 560 peripherals that may be connected indirectly through RCUs [28 RCUs * (10 RFSP(T)s + 5 CRTs + 5 RANKs)]. Each count pair consists of two 16-bit counts (four bytes), one representing the number of print attempts to the specific RFSP Terminal (T) and the second representing the number of resulting errors (or the number of successful entries/errors in the case of a RANK; no SCOPE testing is performed on CRTs in this firmware configuration). Each four byte count pair is transmitted as eight EBCDIC characters for a total of 4,480 characters.

5.2.8 Message Utilization Summary

Table 5-2 illustrates the sequence of all possible input messages.

TABLE 5-2. HOST INPUT MESSAGES/RESPONSES

Preceding Output Message to FDIO	Input Message from FDIO	Resulting Output Message to FDIO
—	Text	RANK Accept, Reject, or Error
Text	Text Acknowledge	—
Invoke Secondary Query Primary	Configuration Status	—
Enable FP Disable FP	Front Panel Status	—
—	Error Status	—
Poll FDIO	Poll Acknowledge	—
SCOPE	SCOPE Response	—

6.0 DATA TRANSFERS OVER PERIPHERAL DEVICE INTERFACE

The PCU and RCU communicate with peripheral devices such as RFSPs, CRTs, and RANK via BCs attached to the PCU or RCU LAN. The BC transmits the text portion of the messages received from the PCU or RCU to the peripheral device over the peripheral device interface. The BC will receive inputs such as RANK entries, protocol control characters, and peripheral status from the peripherals and send them to the PCU or RCU.

Messages are broken down into two categories: operational and setup. All messages transmitted to the peripheral device follow the same format; it is the content of the message text that determines the peripheral device operation, and therefore the category.

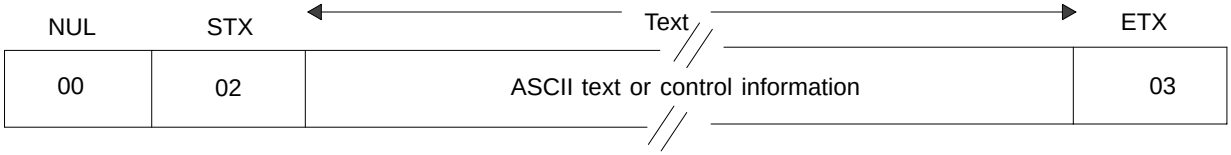
6.1 OPERATIONAL MESSAGES

Operational messages occur during the normal operation of the peripheral device and may be either input or output in nature.

6.1.1 Output Operational Messages

6.1.1.1 Text. Text messages are the result of Host originated Text messages or internal FDIO messages such as diagnostic or error messages. The control unit and BC strips off all control information from the message leaving only the text portion of the message to be sent to the peripheral device. The peripheral device responds by issuing the appropriate protocol characters as defined in appendix B and printing the message.

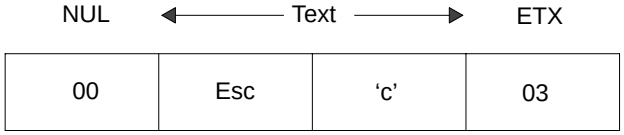
Message Format:



Response from peripheral device: X-OFF
ACK/NAK
X-ON

6.1.1.2 Invoke Diagnostic. The BC may request the printer to perform a diagnostic and internal reset operation by issuing an Invoke Diagnostic message consisting of the following escape sequence: ESC c. If this diagnostic is successful, the peripheral device will transmit an X-ON character to the BC and will clear bit 6 (FAULT) of its status byte (see paragraph 2.3.8). If the diagnostics fails in any way, the peripheral device will set bit 6 of its status byte and will not send an X-ON (or anything else) to the BC. The BC will attempt to (re)establish communication with the peripheral device by continually requesting the peripheral device status on a periodic basis. When an ESC c sequence is sent to an RFSP, it will disable the Offline Self Test and Configuration mode capability.

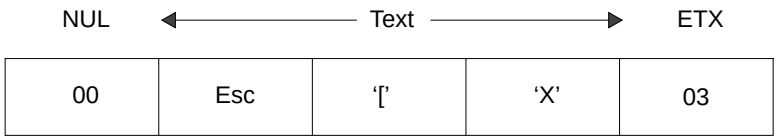
Message Format:



Response from peripheral device: X-ON

6.1.1.3 Request Peripheral Status. The BC may request the peripheral device to send its internal status byte by issuing a Request Peripheral Status message consisting of the following three character escape sequence: Esc [x. See paragraph 2.3.8 for additional information regarding the peripheral status byte.

Message Format:



Response from peripheral device: X-OFF
ACK/NAK
Peripheral status byte
X-ON

6.1.2 Input Operational Text Messages

Input messages received by the BC from a RANK consist of a single ASCII character which is buffered and transmitted to the control unit.

6.2 SETUP MESSAGES

Setup messages typically are sent to the peripheral device following peripheral device interface initialization or after the BC or peripheral device has been restarted. The purpose of these messages is to place the peripheral device into the proper operating mode to assure compatibility with the FDIO system.

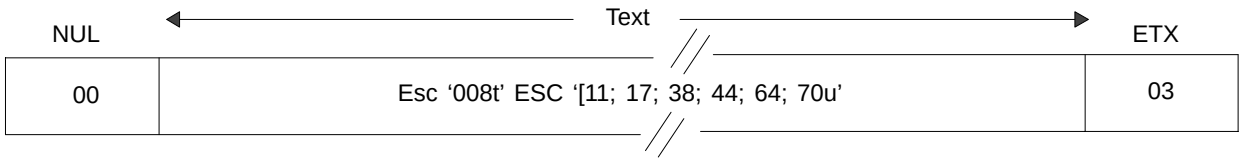
6.2.1 RFSP 1 1/3 Inch Strip

This setup message is sent out to an RFSP attached to a PCU and RFSPs in the oceanic configuration. It performs the following operations:

a. Sets form length for 1 1/3-inch

b. Sets tab stops at 11, 17, 38, 44, 64, and 70

Message Format:



Response from peripheral device: X-OFF
ACK/NAK
X-ON

This message has no effect on a CRT or RANK.

6.2.2 RFSP 1 Inch Strip

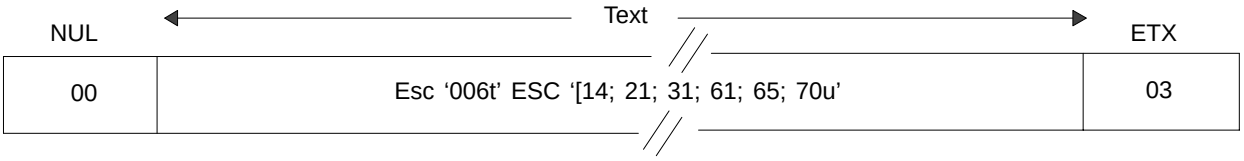
This setup message is sent out to an RFSP attached to a domestic RCU and performs the following operations:

a. Sets form length for 1-inch

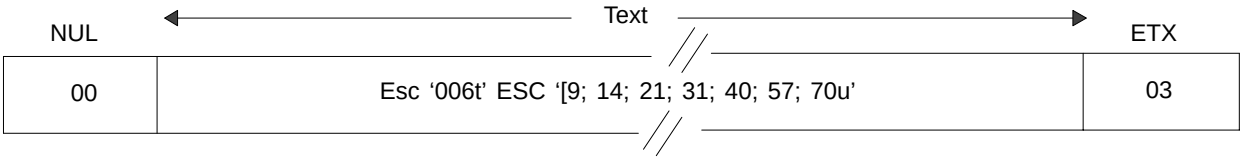
b. Sets tab stops at 14, 21, 31, 61, 65, and 70 [note 1]

c. Sets tab stops at 9, 14, 21, 31, 40, 57, 70 [note 2]

Message Format:



Message Format:



Response from peripheral device: X-OFF
ACK/NAK
X-ON

NOTES

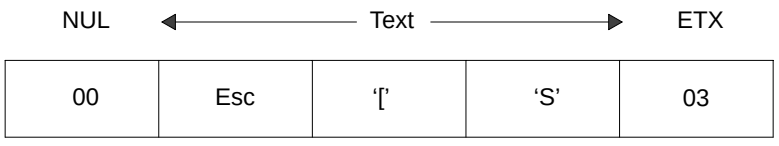
1. These tab settings will be sent to the printer if full strips are requested through RECN on the front panel of the control unit.
2. These tab settings will be sent to the printer if half strips are requested through RECN on the front panel of the control unit.

This message has no effect on a CRT or RANK.

6.2.3 Maint Setup

This setup message is sent out to an RFSP connected to the maintenance channel at a PCU or RCU and enables the front panel configuration mode.

Message Format:



Response from peripheral device: X-OFF
ACK/NAK

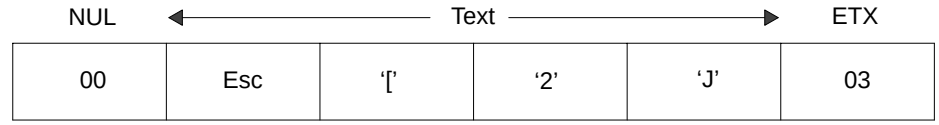
X-ON

This message has no effect on a CRT, RANK, or RFSP (FA 10095/11 and FA 10095/14).

6.2.4 Clear CRT

This message is issued to a CRT and causes lines 1-24 of the CRT display to be cleared (set to blanks).

Message Format:



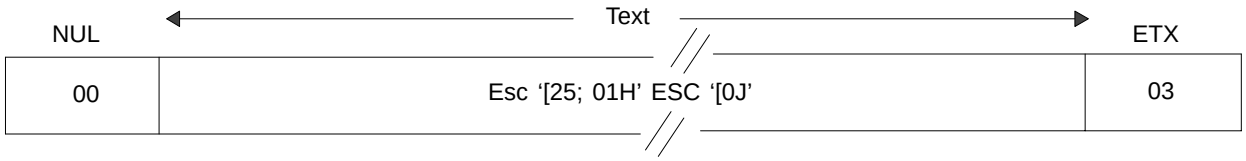
Response from peripheral device: X-OFF
ACK/NAK
X-ON

This message has no effect on an RFSP or RANK.

6.2.5 Erase Line 25

This message is issued to a CRT and causes line 25 of the CRT display to be cleared (set to blanks).

Message Format:



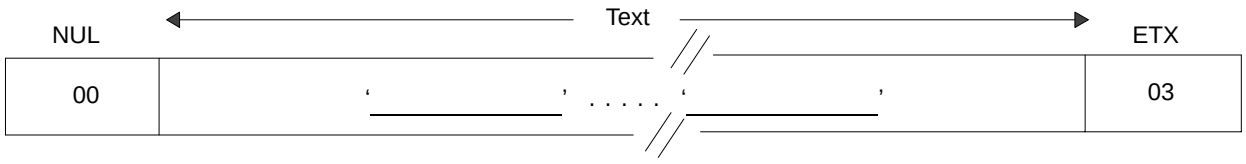
Response from peripheral device: X-OFF
ACK/NAK
X-ON

This message has no effect on an RFSP or RANK.

6.2.6 CRT Divider

This message displays a row of 80 hyphens '-' on the screen of the CRT.

Message Format:



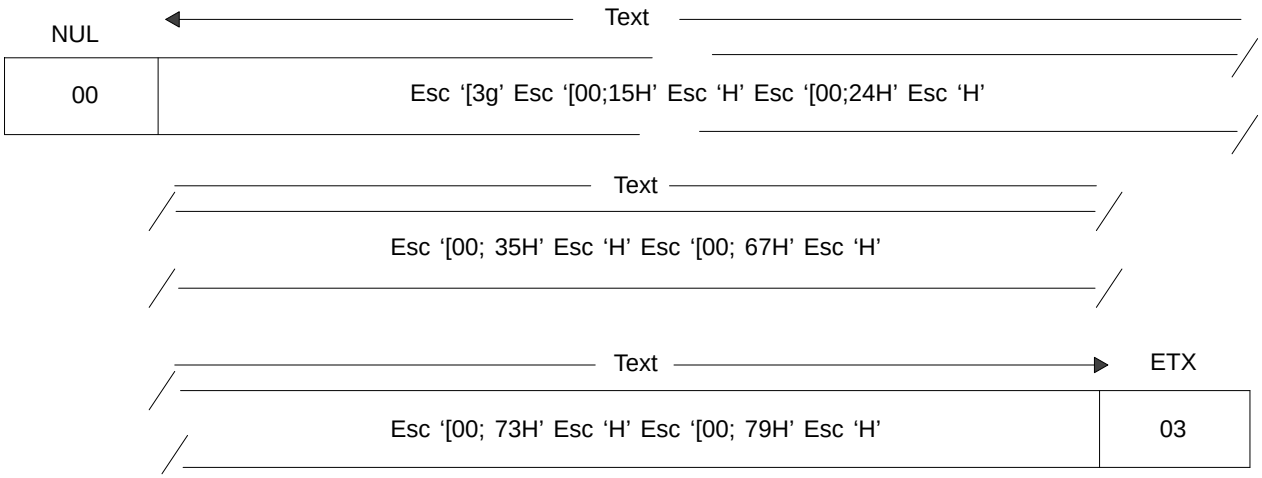
Response from peripheral device: X-OFF
ACK/NAK
X-ON

This setup message is only sent to a CRT and will never be sent to an RFSP or RANK.

6.2.7 Domestic CRT Tab Setup

This setup message is sent to the CRT attached to a doemstic RCU and results in the tabs being set in positions 15, 24, 35, 67, 73, and 79.

Message Format:

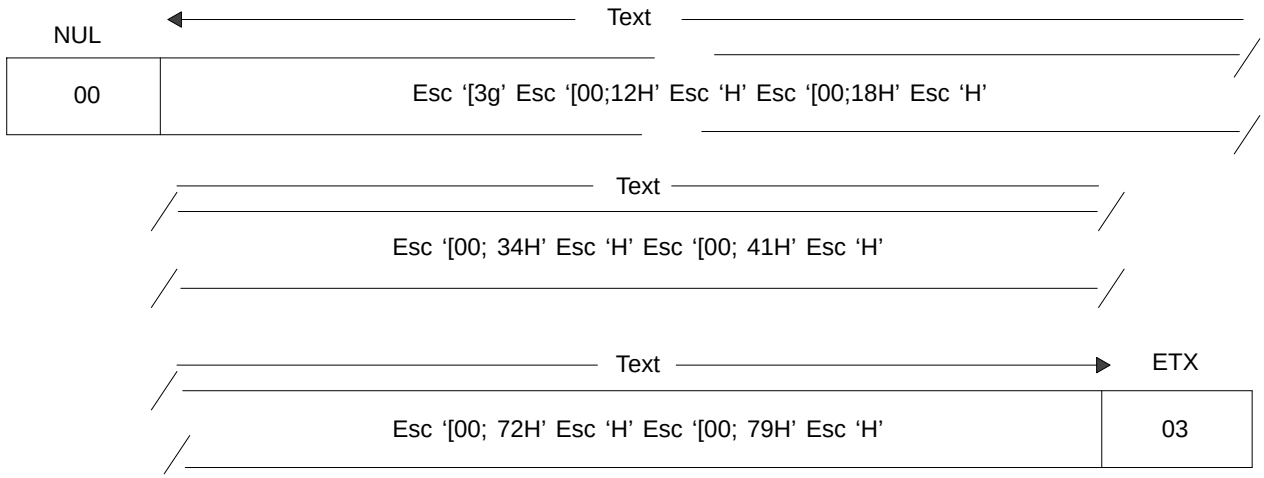


Response from peripheral device: X-OFF
ACK/NAK
X-ON

6.2.8 Oceanic CRT Tab Setup

This setup message is sent to the CRT attached to an oceanic RCU and results in the tabs being set in positions 12, 18, 34, 41, 72 and 79.

Message Format:



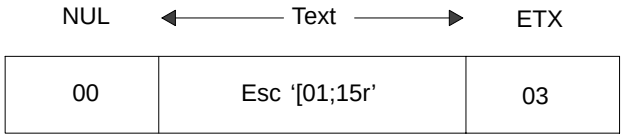
Response from peripheral device: X-OFF
ACK/NAK
X-ON

This message has no effect on an RFSP or RANK.

6.2.9 CRT Scrolling Area (Domestic Configuration Only)

This message is sent to the CRT to setup lines 1 through 15 as a scrolling area.

Message Format:



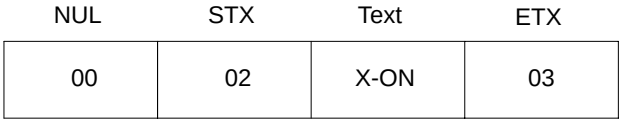
Response from peripheral device: X-OFF
ACK/NAK
X-ON

This message has no effect on an RFSP or RANK.

6.2.10 MWL ON

This message will cause the MWL at the RANK to be illuminated.

Message Format:



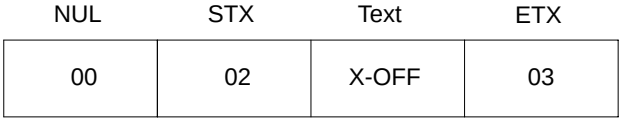
Response from peripheral device: X-OFF
ACK/NAK
X-ON

This message has no effect on a CRT or RFSP.

6.2.11 MWL OFF

This message will cause the MWL at the RANK to be exitinguished.

Message Format:



Response from peripheral device: X-OFF
ACK/NAK
X-ON

This message has no effect on a CRT or RFSP.

7.0 DATA TRANSFER OVER ECHO PORT INTERFACE (PC RCU ONLY)

The PC RCU Peripheral Interface ports can be configured to provide data to other systems such as TDLS, TARDIS Electronic Drop Tube Systems, and Noise Abatement Systems. This interface is a transmit only interface. The PC RCU ignores all data received over this interface. The Echo Port is configured under the Reconfiguration Menu of the PC RCU System Console. The port is configured to receive a copy of the flight data that is addressed to its corresponding RFSP. Each RFSP can be configured to echo up to three echo ports. An echo port can be configured to receive data destined to up to ten printers.

Only flight data text messages as described in section 6.1.1.1 are transmitted over the Echo Port interface. The PC RCU will poll the interface with a NUL character (Hex 00) approximately every two seconds to ensure the interface is operational. No Request Peripheral Status polls are sent because the connected system is not expected to answer. The connected system should not transmit any data over the interface. All data received on this interface is ignored by the PC RCU.

Appendix A

SYSTEM INTERRUPT STRUCTURE

Much of the FDIO I/O operations are performed using hardware interrupts. Figure A-1 diagrams the logical layout of the interrupt structure.

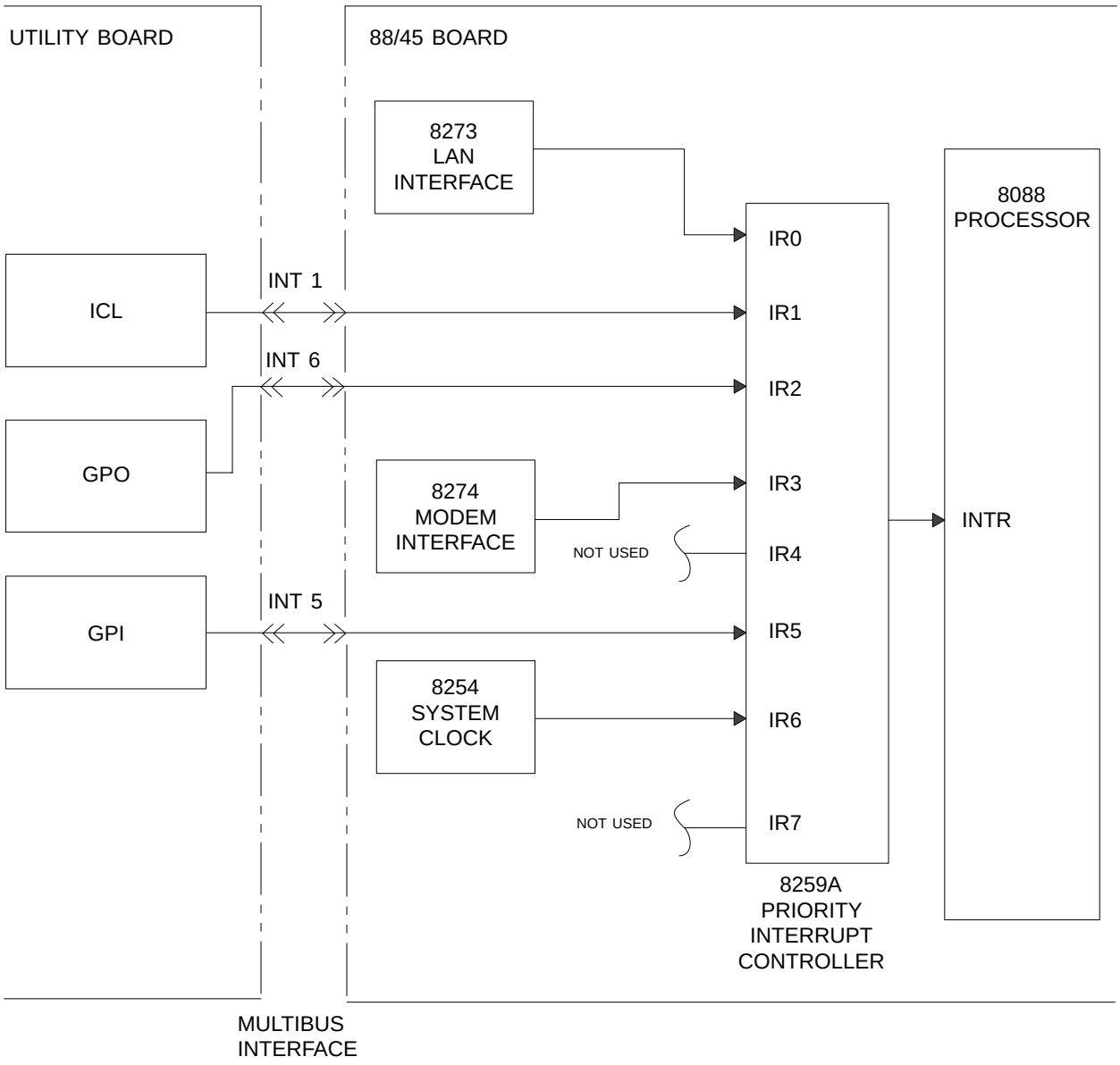


FIGURE A-1. HARDWARE INTERRUPT STRUCTURE

A.1 INTERRUPT STRUCTURE

The 8259A PIC accepts and controls up to eight hardware interrupts connected to its interrupt request lines IR0-IR7. The hardware interrupts are listed below beginning with the highest priority.

IR0 LAN Receive Complete — This interrupt will occur whenever a complete message has been received by the 8273 LAN communications controller. The end of a message will be indicated by the receipt of an End of Poll (EOP) character.

IR1 Intercomputer link — This interrupt will occur whenever a character has been received over the ICL. This interrupt is enabled only at a CCU or PCU.

IR2 GPO — This interrupt is generated whenever the GPO interface channel from the Host has another character to transmit. This interrupt is enabled only at a CCU or PCU.

IR3 Modem — This interrupt occurs whenever the modem channel on an RCU receives a character from the CCU or a character has been transmitted to the CCU. This interrupt is enabled only at an RCU.

IR4 Not used

IR5 GPI — This interrupt occurs whenever a character has been received by the Host via the GPI channel. This interrupt is enabled only for a CCU or PCU.

IR6 System Clock — This interrupt comes from the programmable interval timer and generates an interrupt every 5 msec.

IR7 Not used

The PIC is configured to operate in edge sensitive mode; whenever one of the above interrupt input lines makes a low to high transition, the PIC senses it, latches the request, and locks out other lower priority interrupts. The PIC then activates the single INTR line to the 8088 processor. When the processor is ready to service the interrupt, the PIC places an identification vector onto the data bus which allows the processor to know which of the eight interrupts is pending. Interrupt handling firmware specific to the particular interrupt being serviced is then invoked.

A.2 PIC ADDRESSING

The PIC is addressed as an I/O device and is assigned addresses E0 and E1 hex.

A.3 PIC SETUP

The PIC consists of an 8259A Large Scale Integration (LSI) device and must be initialized as follows:

a. Interrupts will be caused by the rising edge of the interrupt request input line (edge triggered).

b. The starting address of the interrupt vector table in system RAM must be defined as 60 Hex.

c. 8086 (8088) processor mode selected.

d. All interrupts to be temporarily disabled.

The PIC setup is performed by writing to its two control registers as follows:

Command Operation	Command Address	Command Contents (binary)	Command Description
OUTPUT	E0	00010111	Set for edge triggered mode, call interval of 4 bytes, single mode
OUTPUT	E1	60 (hex)	Interrupt vector table begins at address 60 (hex)
OUTPUT	E1	00000001	Set for 8086 processor mode
OUTPUT	E1	11111111	Disable all interrupts

Appendix B

FDIO CHARACTER SET DEFINITION

This appendix defines the characters used by FDIO. Two distinctive sets of definitions exist, an output character set for messages transferred to FDIO from the Host, and an inward character set for messages sent to the Host from FDIO. In addition, the peripheral device interface utilizes special characters required by the communication protocol.

B.1 OUTWARD CHARACTER SET

Outward characters are subdivided into two categories: Those characters sent from the Host over the GPO interface and characters sent over the peripheral device interface.

B.1.1 NAS/FDIO Output Character Set

Table B-1 lists and describes all characters that may be transmitted to FDIO over the GPO interface. The definitions of each column are as follows:

NAS EBCDIC BYTE Column — This column lists all 256 (0 to FF hex) possible bytes the Host is capable of sending.

NAS MNEMONIC Column — This column lists the equivalent EBCDIC symbol. A position marked by backslashes (\\\\\) indicates the GPO byte is invalid and will be rejected if received by FDIO.

ASCII HEX Column — This column shows the ASCII equivalent of the received EBCDIC character. The character is converted from EBCDIC to ASCII by GPO input firmware. A value of FF indicates the byte received from the Host is invalid and will cause FDIO to reject the entire message by raising DSL6.

RFSP/CRT SYMBOL Columns — These columns indicate how the converted ASCII character is displayed by the RFSP or CRT peripheral device. A > preceding a character indicates that the character is large upper case (as opposed to small upper case) character.

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
00	SPACE	20	SPACE	SPACE
01	\\\\\	FF		
02	RED RIBBON [Note]	ESC [31m	RED RIBBON	IGNORE
03	ETX	03	ETX	ETX

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
04	>4	B4	>4	>4
05	HT	09	HT (TAB)	HT (TAB)
06	\\\\\	FF		
07	DEL	7F	DEL	DEL
08	\\\\\	FF		
09	>9	B9	>9	>9
0A	\\\\\	FF		
0B	\\\\\	FF		
0C	\\\\\	FF		
0D	\\\\\	FF		
0E	\\\\\	FF		
0F	\\\\\	FF		
10	\\\\\	FF		
11	\\\\\	FF		
12	BLK RIBBON	ESC [30m	BLK RIBBON	IGNORE
13	\\\\\	FF		
14	\\\\\	FF		
15	CR/LF	0D,0A	CR/LF	CR/LF
16	BK SPACE	08	BK SPACE	BK SPACE
17	IDLE	0	NUL	NUL
18	\\\\\	FF		
19	\\\\\	FF		
1A	\\\\\	FF		
1B	\\\\\	FF		
1C	\\\\\	FF		
1D	\\\\\	FF		
1E	\\\\\	FF		
1F	\\\\\	FF		
20	\\\\\	FF		
21	\\\\\	FF		
22	\\\\\	FF		
23	\\\\\	FF		

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
24	\\\\\	FF		
25	LF	0A	LF	LF
26	EOB	0	NUL	NUL
27	\\\\\	FF		
28	\\\\\	FF		
29	\\\\\	FF		
2A	\\\\\	FF		
2B	\\\\\	FF		
2C	\\\\\	FF		
2D	\\\\\	FF		
2E	\\\\\	FF		
2F	\\\\\	FF		
30	\\\\\	FF		
31	\\\\\	FF		
32	\\\\\	FF		
33	\\\\\	FF		
34	\\\\\	FF		
35	\\\\\	FF		
36	\\\\\	FF		
37	EOT	0	NUL	NUL
38	\\\\\	FF		
39	\\\\\	FF		
3A	\\\\\	FF		
3B	\\\\\	FF		
3C	\\\\\	FF		
3D	\\\\\	FF		
3E	\\\\\	FF		
3F	\\\\\	FF		
40	SPACE	20	SPACE	SPACE
41	\\\\\	FF		
42	\\\\\	FF		
43	\\\\\	FF		

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
44	\\\\\	FF		
45	\\\\\	FF		
46	\\\\\	FF		
47	\\\\\	FF		
48	\\\\\	FF		
49	\\\\\	FF		
4A	ⓟ	0	NUL	NUL
4B	.	2E	.	.
4C	>2	B2	>2	>2
4D	>9	B9	>9	>9
4E	+	2B	+	+
4F	CLR SYM	3C	CLR SYM	CLR SYM
50	[ ]	0	NUL	NUL
51	\\\\\	FF		
52	\\\\\	FF		
53	\\\\\	FF		
54	\\\\\	FF		
55	\\\\\	FF		
56	\\\\\	FF		
57	\\\\\	FF		
58	\\\\\	FF		
59	\\\\\	FF		
5A	←	0	NUL	NUL
5B	DN ARROW	7B	DN ARROW	DN ARROW
5C	*	2A	*	*
5D	>0	B0	>0	>0
5E	>3	B3	>3	>3
5F	ⓠ	0	NUL	NUL
60	-	2D	-	-
61	/	2F	/	/
62	\\\\\	FF		
63	\\\\\	FF		

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
64	\\\\\	FF		
65	\\\\\	FF		
66	\\\\\	FF		
67	\\\\\	FF		
68	\\\\\	FF		
69	\\\\\	FF		
6A	>8	B8	>8	>8
6B	*	2A	*	*
6C	>5	B5	>5	>5
6D	OVC SYM	3E	OVC SYM	OVC SYM
6E	>7	B7	>7	>7
6F	≋	0	NUL	NUL
70	\\\\\	FF		
71	\\\\\	FF		
72	\\\\\	FF		
73	\\\\\	FF		
74	\\\\\	FF		
75	\\\\\	FF		
76	\\\\\	FF		
77	\\\\\	FF		
78	\\\\\	FF		
79	\\\\\	FF		
7A	>4	B4	>4	>4
7B	UP ARROW	7D	UP ARROW	UP ARROW
7C	@	40	@	@
7D	>6	B6	>6	>6
7E	>1	B1	>1	>1
7F	→	0	NUL	NUL
80	\\\\\	FF		
81	>A	41	>A	>A
82	>B	42	>B	>B
83	>C	43	>C	>C

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
84	>D	44	>D	>D
85	>E	45	>E	>E
86	>F	46	>F	>F
87	>G	47	>G	>G
88	>H	48	>H	>H
89	>I	49	>I	>I
8A	\\\\\	FF		
8B	\\\\\	FF		
8C	\\\\\	FF		
8D	\\\\\	FF		
8E	\\\\\	FF		
8F	\\\\\	FF		
90	\\\\\	FF		
91	>J	4A	>J	>J
92	>K	4B	>K	>K
93	>L	4C	>L	>L
94	>M	4D	>M	>M
95	>N	4E	>N	>N
96	>O	4F	>O	>O
97	>P	50	>P	>P
98	>Q	51	>Q	>Q
99	>R	52	>R	>R
9A	\\\\\	FF		
9B	\\\\\	FF		
9C	\\\\\	FF		
9D	\\\\\	FF		
9E	\\\\\	FF		
9F	\\\\\	FF		
A0	\\\\\	FF		
A1	\\\\\	FF		
A2	>S	53	>S	>S
A3	>T	54	>T	>T

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
A4	>U	55	>U	>U
A5	>V	56	>V	>V
A6	>W	57	>W	>W
A7	>X	58	>X	>X
A8	>Y	59	>Y	>Y
A9	>Z	5A	>Z	>Z
AA	\\\\\	FF		
AB	\\\\\	FF		
AC	\\\\\	FF		
AD	\\\\\	FF		
AE	\\\\\	FF		
AF	\\\\\	FF		
B0	\\\\\	FF		
B1	\\\\\	FF		
B2	\\\\\	FF		
B3	\\\\\	FF		
B4	\\\\\	FF		
B5	\\\\\	FF		
B6	\\\\\	FF		
B7	\\\\\	FF		
B8	\\\\\	FF		
B9	\\\\\	FF		
BA	\\\\\	FF		
BB	\\\\\	FF		
BC	\\\\\	FF		
BD	\\\\\	FF		
BE	\\\\\	FF		
BF	\\\\\	FF		
C0	\\\\\	FF		
C1	A	61	A	A
C2	B	62	B	B
C3	C	63	C	C

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
C4	D	64	D	D
C5	E	65	E	E
C6	F	66	F	F
C7	G	67	G	G
C8	H	68	H	H
C9	I	69	I	I
CA	\\\\\	FF		
CB	\\\\\	FF		
CC	\\\\\	FF		
CD	\\\\\	FF		
CE	\\\\\	FF		
CF	\\\\\	FF		
D0	\\\\\	FF		
D1	J	6A	J	J
D2	K	6B	K	K
D3	L	6C	L	L
D4	M	6D	M	M
D5	N	6E	N	N
D6	O	6F	O	O
D7	P	70	P	P
D8	Q	71	Q	Q
D9	R	72	R	R
DA	\\\\\	FF		
DB	\\\\\	FF		
DC	\\\\\	FF		
DD	\\\\\	FF		
DE	\\\\\	FF		
DF	\\\\\	FF		
E0	\\\\\	FF		
E1	\\\\\	FF		
E2	S	73	S	S
E3	T	74	T	T

TABLE B-1. NAS/FDIO OUTPUT CHARACTER SET DEFINITION (Continued)

NAS EBCDIC BYTE	NAS MNEMONIC	ASCII HEX	RFSP SYMBOL	CRT SYMBOL
E4	U	75	U	U
E5	V	76	V	V
E6	W	77	W	W
E7	X	78	X	X
E8	Y	79	Y	Y
E9	Z	7A	Z	Z
EA	\\\\\	FF		
EB	\\\\\	FF		
EC	\\\\\	FF		
ED	\\\\\	FF		
EE	\\\\\	FF		
EF	\\\\\	FF		
F0	0	30	0	0
F1	1	31	1	1
F2	2	32	2	2
F3	3	33	3	3
F4	4	34	4	4
F5	5	35	5	5
F6	6	36	6	6
F7	7	37	7	7
F8	8	38	8	8
F9	9	39	9	9
FA	\\\\\	FF		
FB	\\\\\	FF		
FC	\\\\\	FF		
FD	\\\\\	FF		
FE	\\\\\	FF		
FF	\\\\\	FF		

NOTE

The character 02 hex sent from the Host actually has two definitions. As part of the header field (see paragraph 4.1.1.7), an 02 hex is interpreted as an STX character. When the 02 hex is embedded in the Text field (see paragraph 4.1.1.9), it is interpreted as a red ribbon shift character.

B.1.2 Peripheral Device Character Set

The character set used by the peripheral device interface consists of both printable and control characters.

B.1.2.1 Printable Character Set. The peripheral device uses a modified ASCII character set as listed in table B-2. It should be pointed out that the RFSP and CRT are capable of printing (displaying) a more comprehensive charcter set than the Host can offer.

Note that the lower case alphabetics and numerals are a smaller version of the upper case characters and are not the standard lower case. A > symbol preceding a character indicates that the character is large upper case.

TABLE B-2. PERIPHERAL DEVICE CHARACTER SET

ASCII HEX	ASCII MNEMONIC SPACE	DEFINITION
20	SPACE	
21	!	
22	”	
23	#	
24	$	
25	%	
26	&	
27	’	
28	(	
29	)	
2A	*	
2B	+	
2C	,	
2D	-	
2E	.	
2F	/	
30-39	0 - 9	Small Numerals 0 through 9
3A	:	
3B	;	
3C	○	Clear Weather Symbol

TABLE B-2. PERIPHERAL DEVICE CHARACTER SET (Continued)

ASCII HEX	ASCII MNEMONIC SPACE	DEFINITION
3D	=	
3E	⊕	Cloudy Weather Symbol
3F	?	
40	@	
41-5A	>A - >Z	Large Capital Letters A-Z
5B	[	
5C	\	
5D	]	
5E	^	
5F	_	Underscore
60	‘	
61-7A	A - Z	Small Capital Letters A-Z
7B	↓	Down Arrow
7C	|	
7D	↑	Up Arrow
7E	~	
7F	DEL	
B0-B9	>0 - >9	Large Numerals 0 through 9
BA	¿	Upside Down Question Mark (RANK parity error symbol)
Note	?	Photographic Negative Question Mark (indicates peripheral device parity error)

NOTE

This character is not transmitted to the peripheral device; it is generated by the peripheral device whenever it receives a character with bad parity. This symbol replaces the bad character in the display sequence (CRT) or printed strip (RFSP).

B.1.2.2 Control Characters. The following characters cause control functions to be performed by the peripheral device.

B.1.3 Carriage Return (CR)

The CR character (0D hex) causes the print head or the cursor to move to the beginning of the current line.

B.1.4 Line Feed (LF)

The LF character (0A hex) causes the print head or the cursor to move down by one line.

B.1.5 STX

The STX character (02 hex) will cause an RFSP to position the print head at the First Print Position (FPP) of a new flight strip form. If the print head is already located at this position, no further action is taken. This character is ignored by a CRT or RANK.

B.1.6 Form Feed (FF)

The FF character (0C hex) will cause the RFSP to position the form such that the perforation is aligned with the tear bar. If the form feed is already located at this position, no further action will be taken. This character is ignored by a CRT or RANK.

B.1.7 TAB

The TAB character (09 hex) causes the print head to move in a horizontal manner to the next programmed tab stop. Printable characters following TAB characters will be printed (displayed) in the position immediately following the tab position (i.e., a tab stop at position 14 means the first printable character following the TAB will actually print in position 15). Any number of TAB characters may be present in the message.

B.1.8 ESCAPE

The ESCAPE character (1B hex) is a lead in character and defines the start of an American National Standards Institute (ANSI) Escape sequence. Escape sequences are used to perform such operations as clear screen, absolute cursor positioning, black to red ribbon shifts, etc.

B.2 INWARD CHARACTER SET

Inward characters are subdivided into two categories: Those characters sent to the Host over the GPI interface and input characters generated by a RANK.

B.2.1 NAS/FDIO Input Character Set

Table B-3 lists all legal characters that may be sent to the Host over the GPI interface.

The definitions of each column are as follows:

NAS BYTE HEX Column — This column lists all valid EBCDIC values the Host is capable of receiving.

NAS MNEMONIC Column — This column indicates how the Host interprets the character received.

ASCII HEX Column — This column shows the ASCII equivalent of the transmitted EBCDIC character. The character is converted from ASCII to EBCDIC by GPI firmware.

TABLE B-3. NAS/FDIO INPUT CHARACTER SET

NAS BYTE HEX	NAS MNEMONIC	ASCII HEX
40	SPACE	20
4A	[	5B
4B	.	2E
4D	(	28
4E	+	2B
4F	CLEAR WEATHER	3C
50	&	26
5A	]	5D
5B	DOWN ARROW	7B
5C	*	2A
5D	)	29
5E	;	3B
60	-	2D
61	/	2F
6B	,	2C
6C	%	25
6D	OVERCAST	3E
6F	?	3F
7A	:	3A
7B	UP ARROW	7D
7C	@	40
7D	’	27
7E	=	3D
7F	”	22
C1	A	41
C2	B	42
C3	C	43
C4	D	44
C5	E	45
C6	F	46
C7	G	47
C8	H	48

TABLE B-3. NAS/FDIO INPUT CHARACTER SET (Continued)

NAS BYTE HEX	NAS MNEMONIC	ASCII HEX
C9	I	49
D1	J	4A
D2	K	4B
D3	L	4C
D4	M	4D
D5	N	4E
D6	O	4F
D7	P	50
D8	Q	51
D9	R	52
E2	S	53
E3	T	54
E4	U	55
E5	V	56
E6	W	57
E7	X	58
E8	Y	59
E9	Z	5A
F0	0	30
F1	1	31
F2	2	32
F3	3	33
F4	4	34
F5	5	35
F6	6	36
F7	7	37
F8	8	38
F9	9	39

B.2.2 RANK Input Character Set

Table B-4 defines those characters that originate from a RANK. The groups of columns labeled **NORMAL, SHIFT**, and **CONTROL** represent key stroke interpretations when the key is pressed by itself, the key is pressed together with the shift key or with the control key respectively. Column definitions for columns 2 through 16 are as follows:

Columns 2, 7, and 12 — These columns indicate the actual code generated by the RANK expressed in ASCII hex.

Columns 3, 8, and 13 — These columns indicate the echo code sent to the peripheral device (RFSP or CRT) if appropriate. For example, in the case of a shifted **3**, the RANK would generate a 23 hex (equivalent to an ASCII #), however FDIO firmware will interpret it as a 33 hex (equivalent to an ASCII **3**). It is the 33 hex that will be echoed to the peripheral device.

Columns 4, 9, and 14 — These columns indicate the action that is taken by the FDIO system upon receiving the character from the RANK. An entry not enclosed by angle brackets **< >** is considered data and is echoed. An entry enclosed in angle brackets such as <ENTER> indicates the RANK input is an editing function and may or may not result in an immediate echo response.

Columns 5, 10, and 15 — These columns indicate the EBCDIC sent to the Host (via the GPI port) as a result of the RANK input. Editing inputs may or may not result in a character sent to the Host.

Columns 6, 11, and 16 — These columns reflect interpretation of the characters by the Host.

TABLE B-4. RANK CHARACTER SET DEFINITION

	← NORMAL CHARACTER →					← SHIFT CHARACTER →					← CONTROL CHARACTER →				
RANK KEY	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
OVERCAST	3E	3E	OVERCAST	6D	OVERCAST	3E	3E	OVERCAST	6D	OVERCAST					
1	31	31	1	F1	1	21	31	1	F1	1					
2	32	32	2	F2	2	22	32	2	F2	2					
3	33	33	3	F3	3	23	33	3	F3	3					
4	34	34	4	F4	4	24	34	4	F4	4					
5	35	35	5	F5	5	25	35	5	F5	5					
6	36	36	6	F6	6	26	36	6	F6	6					
7	37	37	7	F7	7	27	37	7	F7	7					
8	38	38	8	F8	8	28	38	8	F8	8					
9	39	39	9	F9	9	29	39	9	F9	9					
0	30	30	0	F0	0	30	30	0	F0	0					
-	2D	2D	-	60	-	3D	2D	-	60	-					
+	2B	2B	+	4E	+	3B	2B	+	4E	+					
ENTER	0D		<ENTER>			0D		<ENTER>			0D		<ENTER>		
ACK	06		<ACK>			06		<ACK>			06		<ACK>		
CLEAR WEATHER	3C	3C	CLEAR WEATHER	4F	CLEAR WEATHER	3C	3C	CLEAR WEATHER	4F	CLEAR WEATHER					
Q	71	71	Q	D8	Q	51	71	Q	D8	Q	11		<LINE INS>		
W	77	77	W	E6	W	57	77	W	E6	W	17				
E	65	65	E	C5	E	45	65	E	C5	E	05		<VER>		
R	72	72	R	D9	R	52	72	R	D9	R	12		<CLR SCRN>		
T	74	74	T	E3	T	54	74	T	E3	T	14		<CHAR INS>		
Y	79	79	Y	E8	Y	59	79	Y	E8	Y	19				
U	75	75	U	E4	U	55	75	U	E4	U	15				
I	69	69	I	C9	I	49	69	I	C9	I	09		<TAB>		
O	6F	6F	O	D6	O	4F	6F	O	D6	O	0F				
P	70	70	P	D7	P	50	70	P	D7	P	10				

TABLE B-4. RANK CHARACTER SET DEFINITION (Continued)

	← NORMAL CHARACTER →					← SHIFT CHARACTER →					← CONTROL CHARACTER →				
RANK KEY	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
@	40	40	@	7C	@	40	40	@	7C	@	00				
BACK SPACE	08		<CURSOR LEFT>			08		<CURSOR LEFT>			08		<CURSOR LEFT>		
LINE INS	11		<LINE INS>			11		<LINE INS>			11		<LINE INS>		
CLR SCRN	12		<CLR SCRN>			12		<CLR SCRN>			12		<CLR SCRN>		
LINE DEL	13		<LINE DEL>			13		<LINE DEL>			13		<LINE DEL>		
BACK TAB	02		<BACK TAB>			02		<BACK TAB>			02		<BACK TAB>		
TAB	09		<TAB>			09		<TAB>			09		<TAB>		
A	61	61	A	C1	A	41	61	A	C1	A	01				
S	73	73	S	E2	S	53	73	S	E2	S	13		<LINE DEL>		
D	64	64	D	C4	D	44	64	D	C4	D	04		<FIELD DEL>		
F	66	66	F	C6	F	46	66	F	C6	F	06		<ACK>		
G	67	67	G	C7	G	47	67	G	C7	G	07				
H	68	68	H	C8	H	48	68	H	C8	H	08		<CURSOR LEFT>		
J	6A	6A	J	D1	J	4A	6A	J	D1	J	0A		<CURSOR DOWN>		
K	6B	6B	K	D2	K	4B	6B	K	D2	K	0B		<CURSOR UP>		
L	6C	6C	L	D3	L	4C	6C	L	D3	L	0C		<CURSOR RIGHT>		
DN ARROW	7B	7B	DN ARROW	5B	DN ARROW	7B	7B	DN ARROW	5B	DN ARROW	7B	7B	DN ARROW	5B	DN ARROW
UP ARROW	7D	7D	UP ARROW	7B	UP ARROW	7D	7D	UP ARROW	7B	UP ARROW	7D	7D	UP ARROW	7B	UP ARROW
NEW LINE	1F		<NEW LINE>			1F		<NEW LINE>			1F		<NEW LINE>		
CHAR INS	14		<CHAR INS>			14		<CHAR INS>			14		<CHAR INS>		
CURSOR UP	0B		<CURSOR UP>			0B		<CURSOR UP>			0B		<CURSOR UP>		

TABLE B-4. RANK CHARACTER SET DEFINITION (Continued)

	← NORMAL CHARACTER →					← SHIFT CHARACTER →					← CONTROL CHARACTER →				
RANK KEY	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CHAR DEL	7F		<CHAR DEL>			7F		<CHAR DEL>			7F		<CHAR DEL>		
BLANK 1	1B					1B					1B				
%	7A	7A	%	E9	%	5A	7A	%	E9	%	1A				
X	78	78	X	E7	X	58	78	X	E7	X	18		<CANCEL>		
C	63	63	C	C3	C	43	63	C	C3	C	03				
V	76	76	V	E5	V	56	76	V	E5	V	16				
B	62	62	B	C2	B	42	62	B	C2	B	02		<BACK TAB>		
N	6E	6E	N	D5	N	4E	6E	N	D5	N	0E				
M	6D	6D	M	D4	M	4D	6D	M	D4	M	0D		<ENTER>		
*	2A	2A	*	5C	*	3A	2A	*	5C	*					
.	2E	2E	.	4B	.	2E	2E	.	4B	.					
/	2F	2F	/	61	/	3F	2F	/	61	/	1C				
BLANK 2	2C					5F					1D				
CURSOR LEFT	08		<CURSOR LEFT>			08		<CURSOR LEFT>			08		<CURSOR LEFT>		
HOME	1E		<HOME>			1E		<HOME>			1E		<HOME>		
CURSOR RIGHT	0C		<CURSOR RIGHT>			0C		<CURSOR RIGHT>			0C		<CURSOR RIGHT>		
SPACE	20	20	SPACE	40	SPACE	20	20	SPACE	40	SPACE	20	20	SPACE	40	SPACE
FIELD DEL	04		<FIELD DEL>			04		<FIELD DEL>			04		<FIELD DEL>		
VER	05		<VER>			05		<VER>			05		<VER>		
CURSOR DOWN	0A		<CURSOR DOWN>			0A		<CURSOR DOWN>			0A		<CURSOR DOWN>		
CANCEL	18		<CANCEL>	18	<CANCEL>	18		<CANCEL>			18		<CANCEL>		

B.3 PERIPHERAL INTERFACE PROTOCOL CHARACTERS

The following characters define the peripheral device interface handshake protocol.

B.3.1 ETX

The peripheral device receives all characters, whether they be printable, control, or escape sequences, and places them into a buffer. An ETX character (03 hex) occupies the last character position of the message. The peripheral device will not commence any operation on the contents of the buffer until the entire message has been received, as evidenced by the receipt of the ETX character.

B.3.2 X-OFF

Upon receipt of the ETX character, the peripheral device sends an X-OFF (13 hex) character to the BC. The X-OFF character informs the BC that the peripheral device has received the ETX indicating the end of the message and has begun processing the message. The only exception is the Request Diagnostic message to which the peripheral device responds only with an X-ON.

B.3.3 ACK

The peripheral device sends an ACK character (06 hex) following the X-OFF character and after the message in the print buffer has been correctly executed. If the message is printable, the ACK indicates it was received without a parity error, the peripheral device is online, there is no abnormality present such as an out of paper or a device fault condition and that the message has been printed (displayed) correctly.

If the message is a request for status or other non-printable message, the ACK response indicates that the peripheral device received the message without a parity error and that it can correctly perform the operation. An ACK is the correct response to a request for status even though the peripheral device is offline or is out of paper.

B.3.4 NAK

The peripheral device sends a NAK (15 hex) character following the X-OFF character if the message received cannot be properly executed. For a printable message, this could be due to a parity error, or if the peripheral device suffers from an out of paper or a device fault condition, or is offline. If a parity error(s) has occurred, the buffer will be printed (displayed) with the character(s) received with bad parity displayed as  The peripheral device will then send an X-ON character to the Host. If an out of paper or device fault condition exists, or the printer is offline, the print buffer will be cleared and the printer will send an X-ON character to the Host without printing the message.

If the message is a request for status or other non-printable message, the NAK response indicates that the message contained a parity error, or a condition exists that will not allow the peripheral device to respond to the message correctly.

If in the process of printing a message, and after the ACK has been sent out, the peripheral device (specifically RFSP) encounters an error condition (i.e., RFSP runs out of paper, is taken offline, or a fault condition occurs), the peripheral device will send a NAK to the Host, clear the print buffer and send the X-ON character.

B.3.5 X-ON

After the peripheral device has processed the message, it will send an X-ON (11 hex) character to the Host to indicate that the operation has been completed and a new message may be sent.

B.3.6 CAN

The CAN (cancel) character (18 hex) causes the peripheral device to clear its buffer without executing it and reset the buffer pointer such that the next character received by the peripheral device is placed in the first buffer position.

Appendix C

FDIO ERROR MESSAGES

The error messages that will be sent to the Host are described in this section. Each error description includes the following:

a. Level — Nonfatal (0) or Fatal (1);

b. Device — Indicates whether a peripheral device is involved, yes or no;

c. NAS Category — 1, 2, or 3 as follows:

Category 1 — Error message sent to Host on each occurrence, as well as front panel and error logger (if enabled) of the affected control unit.

Category 2 — Error message sent to Host only on the first occurrence; error message sent to front panel and error logger (if enabled) of the affected control unit on each occurrence.

Category 3 — Error message sent to the front panel and error logger (if enabled) of the affected control unit, but never to the Host.

d. RCU — Indicates whether an RCU is involved, yes or no;

e. Int Req — Intervention required is appended to these error messages, yes or no;

f. Error Text Message — Shown as it appears in the table.

TABLE C-1. SYSTEM ERROR TABLE, ERRORS 1-85

Error #	Level	Device	NAS Category	RCU	Int Req	Error Text Message
01	1	N	1	N	Y	*PRIMARY LAN FAILED
02	0	N	1	Y	Y	RCU LAN FAILURE
03	0	Y	1	N	N	INDETERMINATE ERROR
04	0	Y	1	Y	N	INDETERMINATE ERROR
05	—	—	—	—	—	RESERVED
06	0	Y	1	Y	Y	PRINTER OUT OF PAPER
07	0	Y	1	N	N	ILLEGAL DEVICE ADDRESS
08	0	Y	1	Y	N	ILLEGAL DEVICE ADDRESS
09	0	Y	1	N	N	MESSAGE TIMED OUT
10	0	Y	1	Y	N	MESSAGE TIMED OUT
11	—	—	—	—	—	RESERVED

TABLE C-1. SYSTEM ERROR TABLE, ERRORS 1-85 (Continued)

Error #	Level	Device	NAS Category	RCU	Int Req	Error Text Message
12	—	—	—	—	—	RESERVED
13	—	—	—	—	—	RESERVED
14	—	—	—	—	—	RESERVED
15	—	—	—	—	—	RESERVED
16	0	Y	1	N	Y	MODEM LINK FAILING
17	0	Y	1	N	Y	BUS CONNECTOR FAILURE
18	0	Y	1	Y	Y	BUS CONNECTOR FAILURE
19	0	N	1	N	Y	ICL CHANNEL FAILURE (PRIMARY)
20	1	N	3	N	Y	ICL CHANNEL FAILURE (SECONDARY)
21	0	N	1	N	Y	PRIMARY FSE TIMED OUT
22	0	N	3	N	Y	SECONDARY FSE TIMED OUT
23	0	N	1	N	N	CONTROL UNIT SWITCH (FORCED)
24	0	N	1	N	N	CONTROL UNIT SWITCH (NORMAL)
25	0	N	2	N	Y	*FSE PRIMARY UNIT FAILURE
26	0	N	2	N	Y	*FSE SECONDARY UNIT FAILURE
27	0	N	1	N	N	CONTROL UNIT SWITCH (F.P.)
28	0	N	2	N	Y	CONTROL UNIT SWITCH (FAILURE)
29	1	N	2	N	Y	*PRIMARY CPU TEST FAILED
30	1	N	2	N	Y	*SECONDARY CPU TEST FAILED
31	—	—	—	—	—	RESERVED
32	1	N	1	N	Y	*PRIMARY ROM FAILURE
33	1	N	3	N	N	SECONDARY ROM FAILURE
34	—	—	—	—	—	RESERVED
35	1	N	1	N	Y	*PRIMARY RAM FAILURE
36	1	N	3	N	N	SECONDARY RAM FAILURE
37	—	—	—	—	—	RESERVED
38	0	N	1	N	Y	ICL CLEAR TO SEND ERROR
39	1	N	2	N	Y	EEPROM FAILURE
40	0	N	2	N	N	*CANNOT DOWNLOAD TO SECONDARY
41	—	—	—	—	—	RESERVED
42	0	N	1	N	N	SWITCH NOT ALLOWED
43	0	N	3	N	N	NAS MESSAGE TOO LONG
44	—	—	—	—	—	RESERVED

TABLE C-1. SYSTEM ERROR TABLE, ERRORS 1-85 (Continued)

Error #	Level	Device	NAS Category	RCU	Int Req	Error Text Message
45	—	—	—	—	—	RESERVED
46	0	N	3	N	N	MODEM TRANSMITTER FAILED
47	0	N	3	N	N	MODEM RECEIVER FAILED
48	0	N	3	N	N	EXCESSIVE ERRORS ON GPI TRANSMITS
49	—	—	—	—	—	RESERVED
50	0	N	3	N	N	UNABLE TO ASSIGN TRANSMITTER (UNIT=2ND)
51	—	—	—	—	—	RESERVED
52	—	—	—	—	—	RESERVED
53	—	—	—	—	—	RESERVED
54	0	N	3	N	N	EXCESSIVE PARITY ERRORS GPO
55	0	N	3	N	N	RCU\CCU CHECKSUM ERROR
56	0	N	3	N	N	PRI\SEC LOOPBACK FAILURE
57	0	N	3	N	N	GPI PARITY ERROR
58	0	N	3	N	N	BAD MESSAGE RECEIVED BY GPO PRIMARY
59	0	N	3	N	N	GPO SECONDARY FAILURE
60	0	N	3	N	N	REJECT MESSAGE RECEIVED FROM PRIMARY
61	0	N	3	Y	N	RCU EEPROM FAILURE
62	—	—	—	—	—	RESERVED
63	0	Y	1	N	N	ILLEGAL PERIPHERAL CONNECTED
64	0	Y	1	N	N	PERIPHERAL IS NOT READY
65	0	Y	1	N	N	PARITY ERROR ENCOUNTERED
66	0	Y	1	N	N	PERIPHERAL IS OFF LINE
67	0	Y	1	N	N	DEVICE FAULT
68	0	Y	1	N	N	BUS CONNECTOR IS BUSY
69	0	N	3	N	Y	WARNING: INVALID CONFIGURATION
70	—	—	—	—	—	RESERVED
71	0	N	3	N	N	INTERNAL FAILURE — SECONDARY DEACTIVATED
72	0	N	3	N	N	INTERNAL FAILURE — PRIMARY AND NO BACKUP
73	—	—	—	—	—	RESERVED
74	0	N	3	N	N	WARNING: FP DISABLED VIA NAS

TABLE C-1. SYSTEM ERROR TABLE, ERRORS 1-85 (Continued)

Error #	Level	Device	NAS Category	RCU	Int Req	Error Text Message
75	0	N	3	N	N	WARNING: FP ENABLED VIA NAS
76	0	N	2	N	N	FSE CABLE INCORRECT OR MISSING
77	0	N	1	N	Y	SPECIAL READ (FORCED SWITCH) FAILURE
78	0	N	1	N	Y	ICL LOOPBACK FAILURE
79	0	Y	1	Y	Y	BUS CONNECTOR CHECKSUM ERROR
80	0	N	3	Y	N	DISK FAILURE
81	0	N	1	Y	Y	MULTI I/O BOARD A FAILURE
82	0	Y	1	Y	Y	UART FAILURE
83	0	Y	1	N	N	DEVICE NOT PRESENT
84	0	N	3	N	N	SYSTEM INITIALIZATION COMPLETE
85	0	N	1	Y	Y	MULTI I/O BOARD B FAILURE

TABLE C-2. SYSTEM ERRORS DEFINED

01 *Primary LAN Failed — NAS C1/FP — **Int Req**

A LAN loop failure has been detected in the primary control unit of a CCU or PCU.

02 RCU LAN Failure — NAS C1/FP — **Int Req**

A LAN loop failure has been detected in an RCU.

03 Indeterminate Error — NAS C1/FP

The LAN firmware has detected a peripheral error in a PCU or CCU. The peripheral device status table is scanned and a Text Ack with Error (type 11) message was returned but no peripheral error status could be determined.

04 Indeterminate Error — NAS C1/FP

The LAN FW has detected a peripheral error in an RCU. The peripheral device status table is scanned and a Text Ack with Error (type 11) message was returned but no peripheral error status could be determined.

05 Reserved

06 Printer Out of Paper — NAS C1/FP — **Int Req**

The LAN firmware has detected an **out of paper** bit set in the peripheral status word of a PCU or RCU.

TABLE C-2. SYSTEM ERRORS DEFINED (Continued)

07	Illegal Device Address — NAS C1/FP The RCU detects an invalid destination.
08	Illegal Device Address — NAS C1/FP The CCU/PCU detects an invalid destination.
09	Message Timed Out — NAS C1/FP A CCU/PCU associated peripheral fails to acknowledge a message within an allotted time.
10	Message Timed Out — NAS C1/FP An RCU associated peripheral fails to acknowledge a message within an allotted time.
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Modem Link Failing — NAS C1/FP — **Int Req** The CCU BC firmware detects a permanent time-out condition due to hardware/TELephone COmpany (TELCO) problems.
17	Bus Connector Failure — NAS C1/FP — **Int Req** The LAN firmware examined the CCU/PCU bus connector status word and found either: a. BC not ready b. BC checksum error
18	Bus Connector Failure — NAS C1/FP — **Int Req** The LAN firmware examined the RCU bus connector status word and found either: a. BC not ready b. BC checksum error
19	ICL Channel Failure (Primary) — NAS C1/FP — **Int Req** The Inter Computer Link firmware has detected a time-out or data mismatch condition on ICL channel A and channel B loopback tests.

TABLE C-2. SYSTEM ERRORS DEFINED (Continued)

20	ICL Channel Failure (Secondary) — NAS C3/FP — **Int Req** The Inter Computer Link firmware has detected a time-out or data mismatch condition on ICL channel A and channel B loopback tests.
21	Primary FSE Timed Out — NAS C1/FP — **Int Req** Fail Safe Electronics (FSE) Watchdog timer is not updated in time by the primary unit.
22	Secondary FSE Timed Out — NAS C3/FP — **Int Req** FSE Watchdog timer is not updated in time by the secondary unit.
23	Control Unit Switch (Forced) — NAS C1/FP NAS raised GPI Device Control Line 4 forcing a control unit switch.
24	Control Unit Switch (Normal) — NAS C1/FP NAS initiated a control unit switch via a Type 30 Invoke Backup message.
25	*FSE Primary Unit Failure — NAS C2/FP — **Int Req** The FSE of the secondary control unit detects a failure in the primary. Secondary switches to primary, deactivates the old primary, and operates as a single unit.
26	*FSE Secondary Unit Failure — NAS C2/FP — **Int Req** The FSE of the primary control unit detects a failure in the secondary. The primary deactivates the old secondary and operates as a single unit.
27	Control Unit Switch (F.P.) — NAS C3/FP A front panel control unit switch has been processed.
28	Control Unit Switch (FAILURE) — NAS C2/FP — **Int Req** FSE detected the control unit to be unavailable during power up. Control unit operation is deactivated.
29	*Primary CPU Test Failed — NAS C2/FP — **Int Req** Primary unit detected an internal failure and deactivated. If available, the secondary unit is brought online. If the secondary is unavailable, error message 72 (Internal Failure — Primary and No Backup) is displayed on the front panel.

TABLE C-2. SYSTEM ERRORS DEFINED (Continued)

30	*Secondary CPU Test Failed — NAS C2/FP — **Int Req** The secondary control unit detects a failure in the primary, however the primary has not failed which indicates the secondary has failed. The secondary control unit deactivates and Error Message 71(Internal Fail — Secondary Deactivated) is posted to the front panel.
31	Reserved
32	*Primary ROM Failure — NAS C1/FP — **Int Req** A calculated checksum failure has been detected in the primary control unit (or RCU) ROM by background diagnostics.
33	Secondary ROM Failure — NAS C3/FP A calculated checksum failure has been detected in the secondary control unit ROM by background diagnostics.
34	Reserved
35	*Primary RAM Failure — NAS C1/FP — **Int Req** A compliment/exclusive OR failure has been detected in the primary control unit (or RCU) RAM by background diagnostics.
36	Secondary RAM Failure — NAS C3/FP A compliment/exclusive OR failure has been detected in the secondary control unit RAM by background diagnostics.
37	Reserved
38	*ICL Clear To Send Error — NAS C1/FP — **Int Req** ICL firmware in the primary control unit detects Clear To Send (CTS) signal missing. Could be caused by the ICL cable missing or improperly seated.
39	EEPROM Failure — NAS C2/FP — **Int Req** The site configuration data has been erased from the EEPROM. The EEPROM needs to be reconfigured through the RECN button on the front panel.
40	*Cannot Down Load to Secondary — NAS C2/FP ICL failed to establish a download mode which negates message synchronization between primary and secondary control units.
41	Reserved

TABLE C-2. SYSTEM ERRORS DEFINED (Continued)

42 Switch Not Allowed — NAS C1/FP

a. A front panel switch request was entered from a secondary control unit.

b. A front panel switch request was entered from a primary control unit and no secondary is online.

c. Primary control unit detects an ICL failure during a requested switch.

43 NAS Message Too Long — NAS C3/FP

Primary Control Unit detects message overflow and signals the NAS with DSL5. NAS aborts the current message.

44 Reserved

45 Reserved

46 Modem Transmitter Failed — NAS C3/FP

Transmissions to the CCU from the RCU have been attempted two times and failed.

47 Modem Receiver Failed — NAS C3/FP

The RCU attempted to transmit a message three times and failed.The RCU failed to receive the ADCCP link-level acknowledgement from the CCU.

48 Excessive Errors on GPI Transmits — NAS C3/FP

Excessive errors have occurred on the same GPI input message. Works in conjunction with Error Message 57. DSL3 (Request Resend) line has been raised on the successive transmissions of the message.

49 Reserved

50 Unable To Assign Transmitter (Unit=2nd) — NAS C3/FP

a. When reported by primary, indicates secondary failed to assume primary status on a control unit switch.

b. When reported by the secondary, indicates the transmitter function was not acquired.

51 Reserved

52 Reserved

53 Reserved

TABLE C-2. SYSTEM ERRORS DEFINED (Continued)

54	Excessive Parity Errors GPO — NAS C3/FP Two successive parity errors detected on the same message. FDIO GPO interface logic reinitialized.
55	RCU/CCU Checksum Error — NAS C3/FP CCU computed checksum does not match checksum stored in RANK message.
56	Pri/Sec Loopback Failure — NAS C3/FP Internal Control Unit test pattern data mismatch or parity error detected in **primary** control unit.
57	GPI Parity Error — NAS C3/FP GPI loopback test for parity has failed. This test is run as a result of DSL3 being raised.
58	Bad Message Received By GPO Primary — NAS C3/FP Primary Control Unit tests for invalid message format, raises DSL6 (request resend) to NAS when message does not: a. end with ETX, b. have minimum message length of 12 bytes, c. contain STX in header, or d. contain all legal characters in message.
59	GPO Secondary Failure — NAS C3/FP Primary/Secondary checksum mismatch. DSL6 raised to NAS which requests NAS to resend the message to the control unit.
60	Reject Message Received from Primary — NAS C3/FP Primary control unit informed secondary to reject the last message. (Used in conjunction with Error Message 59.)
61	RCU EEPROM Failure — NAS C3/FP The site configuration data has been erased from the EEPROM. The EEPROM needs to be reconfigured through the RECN button on the front panel.
62	Reserved

TABLE C-2. SYSTEM ERRORS DEFINED (Continued)

63	Illegal Peripheral Connected — NAS C1/FP The bus connector status indicates an illegal peripheral is connected. i. e., an RFSP connected to a BC with a RANK address.
64	Peripheral Is Not Ready — NAS C1/FP The PCU/RCU bus connector status word indicates the attached peripheral is not ready during the last attempted access.
65	Parity Error Encountered — NAS C1/FP The bus connector peripheral status reports a parity error has occurred during the last peripheral data transfer.
66	Peripheral Is Off Line — NAS C1/FP The bus connector peripheral status reports an off line condition existed during the last attempted peripheral access.
67	Device Fault — NAS C1/FP The bus connector peripheral status reports a device fault, i.e., Headjam, condition existed during the last attempted peripheral access.
68	Bus Connector is Busy Too Long — NAS C1/FP BC status indicates busy after two retries during a specified time parameter, indicating the busy condition has been in effect too long.
69	Warning: Invalid Configuration — NAS C3/FP — **Int Req** The RCU detected minimum configuration requirements of at least one RANK and one RFSP or CRT not available.
70	Reserved
71	Internal Failure — Secondary Deactivated — NAS C3/FP An internal failure is detected in the secondary control unit. The unit deactivates itself. (See Error Message 30.)
72	Internal Failure — Primary and No Backup — NAS C3/FP Primary unit detects an internal failure with no complimentary control unit to switch to. (See Error Message 29.)
73	Reserved

TABLE C-2. SYSTEM ERRORS DEFINED (Continued)

74	Warning: FP Disabled Via NAS — NAS C3/FP A Front Panel Disable command has been received from NAS.
75	Warning: FP Enabled Via NAS — NAS C3/FP A Front Panel Enable command has been received from NAS.
76	FSE Cable Incorrect or Missing — NAS C2/FP
77	Special Read (Forced Switch) Failure — NAS C1/FP — **Int Req** NAS has detected a solid error (undefined) on the FDIO/NAS interface operation and issued a forced switch to the secondary.
78	ICL Loopback Failure — NAS C1/FP — **Int Req** A time-out or data mismatch was detected when ICL channels A and B were operated in loopback mode. (Loopback mode verifies control unit operation without a redundant control unit.)
79	Bus Connector Checksum Error — NAS C1/FP — **Int Req** The checksum that was calculated by the BC is different than the checksum stored in the message. If a backup device is specified, the message will be rerouted. If no backup or reroute is unsuccessful, a NAK will be generated.

TABLE C-3. PC-RCU SYSTEM ERRORS DEFINED

04	Indeterminate Error — NAS C1/SM The PC-RCU has detected a peripheral error. The peripheral device status table is scanned and a Text Ack with Error (type 11) message was returned but no peripheral error status could be determined.
06	Printer Out of Paper — NAS C1/SM — **Int Req** The PC-RCU software has detected an **out of paper** bit set in the status word returned from a printer.
07	Illegal Device Address — NAS C1/SM The PC-RCU detects an invalid destination.
09	Message Timed Out — NAS C1/SM A PC-RCU associated peripheral fails to acknowledge a message within an allotted time.

TABLE C-3. PC-RCU SYSTEM ERRORS DEFINED (Continued)

46 Modem Transmitter Failed — NAS C3/SM

Transmissions to the CCU from the PC-RCU have been attempted two times and failed.

47 Modem Receiver Failed — NAS C3/SM

The PC-RCU attempted to transmit a message three times and failed. The PC-RCU failed to receive the ADCCP link-level acknowledgement from the CCU.

63 Illegal Peripheral Connected — NAS C1/SM

The device type returned from the peripheral is not compatible with the address (device number) it is associated with as per the RECN table. i.e., an RFSP configured to a RANK device number (16-20).

64 Peripheral Is Not Ready — NAS C1/SM

The PC-RCU device status word indicates the attached peripheral is not ready during the last attempted access.

65 Parity Error Encountered — NAS C1/SM

The peripheral status returned indicates a parity error has occurred during the last peripheral data transfer.

66 Peripheral Is Off Line — NAS C1/SM

The peripheral status indicates an offline condition existed during the last attempted peripheral access.

67 Device Fault — NAS C1/SM

The perpheral status reports a device fault, i.e., Headjam condition existed during the last attempted peripheral access.

80 Disk Failure — NAS C3/FP

The disk failure message signifies a problem reading from or writing to disk.

81 Multi I/O Board A Failure — NAS C1/FP — **Int Req**

All Universal Asynchronous Receiver Transmitters (UART) on the Peripheral Interface Board-A.

82 UART Failure — NAS C1/FP — **Int Req**

A problem exists with one of the UART chips on the Peripheral Interface board.

TABLE C-3. PC-RCU SYSTEM ERRORS DEFINED (Continued)

83	Device Not Present — NAS C1/FP
	The device solicited was not found in the PC-RCU configuration table.
84	System Initialization Complete — NAS C3/FP
	Signifies successful initialization of PC-RCU.
85	Multi I/O Board B Failure — NAS C1/FP — **Int Req**
	All UARTs on the Peripheral Interface Board-B have failed.

Appendix D

FDIO MASTER ACRONYM GLOSSARY

ABBREVIATIONS

ACRONYM	DEFINITION
ABM	Asynchronous Balanced Mode
ADCCP	Advanced Data Communications Control Protocol
ANSI	American National Standards Institute
ARTCC	Air Route Traffic Control Center
ARTS	Automated Radar Terminal System
ASCII	American Standard Code For Information Interchange
ASM-86	The assembly language use by the Intel 8086 family of processors.
BC	Bus Connector
BITE	Built-In Test Equipment
bps	bits-per-second
CCB	Configuration Control Board (See SCCB)
CCC	Central Computer Complex
CCU	Central Control Unit
CDR	Critical Design Review (See FTAR)
CLINO	Contractual Line Item Number
CM	Configuration Management
CMI	Configuration Management Identifier Number
CMID	Configuration Management ID
CPFS	Computer Program Functional Specification
CPI	Computer Program Item

CPM	Computer Program Module
CPSM	Computer Program Subsystem Module
CPTR	Computer Program Technical Report
CPU	Computer Processing Unit
CQCSP	Computer Quality Control System Plan/Program
CR	Carriage Return
CRC	Cyclical Redundancy Check (same as FCS)
CRT	Cathode Ray Tube (a monitor)
CSQPP	Computer Software Quality Program Plan
CTS	Clear to Send
CU	Control Unit
DCL	Device Control Lines
DMA	Direct Memory Access
DOT	Department Of Transportation
DS	Data Segment Register
DSL	Device Status Line
EBCDIC	Extended Binary-Coded Decimal Information Code
ECO	Engineering Change Order
EEROM	Electrically Erasable Read Only Memory (nonvolatile)
EO	Engineering Order
EOM	End of Message
EOP	End of Poll
EPROM	Electrically Programmable Read Only Memory (nonvolatile, erasable by ultraviolet light)
FAA	Federal Aviation Administration
FCL	Functional Capabilities List
FCS	Frame Check Sequence (same as CRC)
FDEP	Flight Data Entry and Printout
FDIO	Flight Data Input/Output

FDN	Firmware Development Notebooks
FF	Form Feed
FM	Firmware Manager
FORTRAN-86	ANSI 1977 standard version of FORTRAN used by the Intel 8086 family of processors
FPP	First Print Position
FSDR	Final Software Design Review
FSE	Fail Safe Electronics (Hardware)
FSG	Federal Systems Group
FSM	Fail Safe Module (Firmware)
FSP	Flight Strip Printer
FTAR	Final Technical Approach Review (same as CDR)
GFE	Government Furnished Equipment
GPI	General Purpose Input (Host input channel)
GPO	General Purpose Output (Host output channel)
High	High logic level is > 2.5 volts D.C.
I	Information frame
IBM	International Business Machine
ICE	In Circuit Emulator
ICL	Intercomputer Link
ID	Identification
I/O	Input/Output
iSBC	Intel Single Board Computer series
ITAR	Initial Technical Approach Review (same as PDR)
LAN	Local Area Network
Low	Low logic level < 0.7 volts D.C.
LF	Line Feed
LSB	Least Significant Bit, also referred to as bit 0
LSI	Large Scale Integration

MDS	(Intel's) Microcomputer Development System
MSB	Most Significant Bit, also referred to as bit 7 for 8- bit data or bit 15 for 16-bit data
MSec	Millisecond
MWL	Message Waiting Light
NAS	National Airspace System
NRM	Normal Response Mode
NRZ	Non Return to Zero, a method of encoding serialized data
OCPD	Overall Computer Program Description
PAMRI	Peripheral Adapter Module Replacement Item (Hardware at Host)
PCU	Printer Control Unit
PDP	Program Development Plan (Volume VI, Appendix A)
PDR	Preliminary Design Review (see FTAR)
PDS	Program Design Specification
PDST	Peripheral Device Status Table
PIC	Priority Interrupt Controller (8259A)
PM	Program Manager
PPI	Parallel Peripheral Interface (8255A)
PROM	Programmable Read Only Memory
QC	Quality Control
QMG	Quality Management Group
RAM	Random Access Memory (volatile)
RANK	Replacement Alphanumeric Keyboard
REJ	Reject
RCU	Remote Control Unit
RFSP	Replacement Flight Strip Printer
RFSP(E)	Replacement Flight Strip Printer En Route
RFSP(T)	Replacement Flight Strip Printer Terminal
RNR	Response Not Ready

ROM	Read Only Memory
RR	Response Ready
SABM	Set Asynchronous Balanced Mode
SCCB	Software Configuration Control Board
SCCD	Software Configuration Control Directive
SCCF	Software Configuration Control Facilities
SCCR	Software Configuration Change Request
SCM	Software Configuration Management
SCOPE	System Checkout of Peripheral Equipment
SCR	System Coordination Report
SDD	Software Design Data
SDP	Software Development Plan (Same as SDSM)
SDSM	Software Development Standard Manual (Same as SDP)
SE	Systems Engineer
SICD	Software Interface Control Document
SM	Subsystem Module
SMC	Systems Maintenance Channel
SMDR	Subsystem Module Development Report
SMMC	Systems Maintenance Monitor Console
SNRM	Set Normal Response Mode
SPB	Software Problem Board
SQA	Software Quality Assurance
SQAE	Software Quality Assurance Engineer
SQM	Software Quality Management
SPR	Software Problem Report
SPRB	Software Problem Review Board
SRTM	Software Requirements Traceability Matrix
STR	System Trouble Report

TAD	Task Assignment Description
TCRM	Test Case to Requirements Matrix
TELCO	TELephone COmpany
T&M	Test and Maintenance
UA	Unnumbered Acknowledgment
UART	Universal Asynchronous Receiver Transmitters
UDF	Unit Development Folders
UT	Unit Test
UTR	Unit Test Review
XID	Exchange ID

Appendix E

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